SYC SEMICONDUCTORES Y COMPONENTES

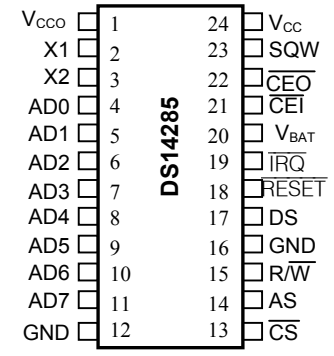
DS14285/DS14287
Real-Time Clock with NV RAM Control Control

FEATURES

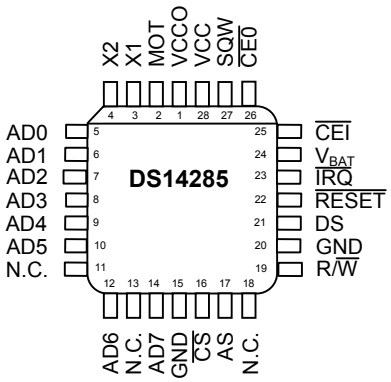
- **Direct Replacement for IBM AT Computer Clock/Calendar**
- **Functionally Compatible with the DS1285/DS1287**
- **Available as Chip (DS14285, DS14285S, or DS14285Q) or Stand-Alone Module with Embedded Lithium Battery and Crystal (DS14287)**
- **Automatic Backup Supply and Write Protection to Make External SRAM Nonvolatile**
- **Counts Seconds, Minutes, Hours, Days, Day of the Week, Date, Month, and Year with Leap Year Compensation Valid Up to 2100**
- **Binary or BCD Representation of Time, Calendar, and Alarm**
- **12- or 24-Hour Clock with AM and PM in 12-Hour Mode**
- **Daylight Saving Time Option**
- **Multiplex Bus for Pin Efficiency**
- **Interfaced with Software as 128 RAM Locations**
  14 Bytes of Clock and Control Registers
  114 Bytes of General Purpose RAM
- **Programmable Square-Wave Output Signal**
- **Bus-Compatible Interrupt Signals ($\overline{IRQ}$)**
- **Three Interrupts are Separately Software-Maskable and Testable**
  Time-of-Day Alarm Once/Second to Once/Day
  Periodic Rates from 122µs to 500ms
  End of Clock Update Cycle
- **Optional Industrial Temperature Version Available: DS14285 DIP, SO, and PLCC**

PIN CONFIGURATIONS

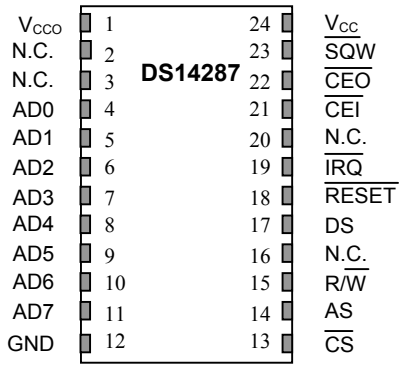
TOP VIEW



DIP/SO



PLCC



Encapsulated Package

ORDERING INFORMATION

PART	TEMP RANGE	VOLTAGE (V)	PIN-PACKAGE	TOP MARK*
DS14285	0°C to +70°C	5.0	24 DIP (0.600″)	DS14285
DS14285+	0°C to +70°C	5.0	24 DIP (0.600″)	DS14285
DS14285N	-40°C to +85°C	5.0	24 DIP (0.600″)	DS14285N
DS14285N+	-40°C to +85°C	5.0	24 DIP (0.600″)	DS14285N
DS14285Q	0°C to +70°C	5.0	28 PLCC	DS14285Q
DS14285Q+	0°C to +70°C	5.0	28 PLCC	DS14285Q
DS14285QN	-40°C to +85°C	5.0	28 PLCC	DS14285QN
DS14285QN+	-40°C to +85°C	5.0	28 PLCC	DS14285QN
DS14285S	0°C to +70°C	5.0	24 SO (0.300″)	DS14285S
DS14285S+	0°C to +70°C	5.0	24 SO (0.300″)	DS14285S
DS14285SN	-40°C to +85°C	5.0	24 SO (0.300″)	DS14285SN
DS14285SN+	-40°C to +85°C	5.0	24 SO (0.300″)	DS14285SN
DS14285SN/T&R	-40°C to +85°C	5.0	24 SO (0.300″)/Tape & Reel	DS14285SN
DS14285SN+T&R	-40°C to +85°C	5.0	24 SO (0.300″)/Tape & Reel	DS14285SN
DS14285S/T&R	0°C to +70°C	5.0	24 SO (0.300″)/Tape & Reel	DS14285S
DS14285S+T&R	0°C to +70°C	5.0	24 SO (0.300″)/Tape & Reel	DS14285S
DS14287	0°C to +70°C	5.0	24 EDIP (0.740″)	DS14287
DS14287+	0°C to +70°C	5.0	24 EDIP (0.740″)	DS14287

+ Denotes a lead-free/RoHS-compliant device.
** A "+" anywhere on the top mark denotes a lead-free/RoHS-compliant device. An "N" denotes an industrial temperature grade device.*

PIN DESCRIPTION

AD0-AD7 - Multiplexed Address/Data Bus
NC - No Connection
MOT - Bus Type Select (DS14285Q only)
$\overline{CS}$ - Chip Select
AS - Address Strobe
R/$\overline{W}$ - Read/Write Input
DS - Data Strobe
$\overline{RESET}$ - Reset Input
$\overline{IRQ}$ - Interrupt Request Output
SQW - Square Wave Output
V_{CC} - +5V Supply
GND - Ground
V_{CCO} - RAM Power Supply Output
$\overline{CEI}$ - RAM Chip Enable In
$\overline{CEO}$ - RAM Chip Enable Out
X1, X2 - 32.768 kHz Crystal Connections
V_{BAT} - +3V Battery Input

DETAILED DESCRIPTION

The DS14285/DS14287 Real Time Clock with NVRAM Control provides the industry standard DS1287 clock function with the additional feature of providing nonvolatile control for an external SRAM. Functions include a nonvolatile time-of-day clock, alarm, 100-year calendar, programmable interrupt, square wave generator, and 114 bytes of nonvolatile static RAM. For the DS14287 a lithium energy source, quartz crystal, and write protection circuitry are contained within a 24-pin dual in-line package. The DS14285 requires an external quartz crystal connected to the X1 and X2 pins as well as an external energy source connected to the V_{BAT} pin. A standard 32.768 kHz quartz crystal can be directly connected to the DS14285 via pins 1 and 2 (X1, X2). The crystal selected for use should have a specified load capacitance (C_L) of 6 pF. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real-time Clocks."

The DS14285/DS14287 uses its backup energy source and battery-backup controller to make a standard CMOS static RAM nonvolatile during power-fail conditions. During power fail, the DS14285/DS14287 automatically write-protects the external SRAM and provides a V_{CC} output sourced from its internal battery.

For the DS14287 the internal lithium cell is electrically isolated from the clock and memory when shipped from the factory. This isolation is removed after the first application of $V_{CC,}$ allowing the lithium cell to provide data retention to the clock, internal RAM, V_{CCO} and $\overline{CEO}$ on subsequent power-downs. Care must be taken after this isolation has been broken to avoid inadvertently discharging the lithium cell through the V_{CCO} and $\overline{CEO}$ pins.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS14285/DS14287. The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +5 volt input.

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the real time clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

AD0-AD7 (Multiplexed Bi-directional Address/Data Bus) - Multiplexed buses save pins because address information and data information time-share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS14285/DS14287 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the DS14285/DS14287 latches the address from AD0 to AD6. Valid write data must be present and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle the DS14285/DS14287 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as $\overline{RD}$ transitions high in the case of Intel timing.

MOT (Mode Select) - The MOT pin offers the flexibility to choose between to bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 KΩ. This pin is on the DS14285Q only.

AS (Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the DS14285/DS14287.

DS (Data Strobe or Read Input) - For the DS14285Q the DS/$\overline{RD}$ pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the DS14285Q is to drive the bidirectional bus. In write cycles the trailing edge of DS causes the DS14285Q to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read($\overline{RD}$). $\overline{RD}$ identifies the time period when the DS14285Q drives the bus with read data. The $\overline{RD}$ signal is the same definition as the Output Enable ($\overline{OE}$) signal on a typical memory.

The DS14285, DS14285S and DS14287 do not have a MOT pin and therefore operate only in Intel bus timing mode.

R/$\overline{W}$ (Read/Write Input) - The R/$\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, R/$\overline{W}$ is at a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high. A write cycle is indicated when R/$\overline{W}$ is low during DS.

When the MOT pin is connected to GND for Intel timing, the R/$\overline{W}$ signal is an active low signal called $\overline{WR}$. In this mode the R/$\overline{W}$ pin has the same meaning as the Write Enable signal ($\overline{WE}$) on generic RAMs.

$\overline{CS}$ (Chip Select Input) - The Chip Select signal must be asserted low for a bus cycle in the DS14285/DS14287 to be accessed. $\overline{CS}$ must be kept in the active state during DS for Motorola timing and during $\overline{RD}$ and $\overline{WR}$ for Intel timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur. When V_{CC} is below 4.25 volts, the DS14285/DS14287 internally inhibits access cycles by internally disabling the $\overline{CS}$ input. This action protects both the real time clock data and RAM data during power outages.

$\overline{IRQ}$ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the DS14285/DS14287 that can be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin the processor program normally reads the C register. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pull-up resistor.

$\overline{\text{RESET}}$ (Reset Input) - The $\overline{\text{RESET}}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{\text{RESET}}$ pin can be held low for a time in order to allow the power supply to stabilize. The amount of time that $\overline{\text{RESET}}$ is held low is dependent on the application. However, if $\overline{\text{RESET}}$ is used on power-up, the time $\overline{\text{RESET}}$ is low should exceed 200 ms to make sure that the internal timer that controls the DS14285/DS14287 on power-up has timed out. When $\overline{\text{RESET}}$ is low and V_{CC} is above 4.25 volts, the following occurs:

A. Periodic Interrupt Enable (PEI) bit is cleared to 0.
B. Alarm Interrupt Enable (AIE) bit is cleared to 0.
C. Update Ended Interrupt Flag (UF) bit is cleared to 0.
D. Interrupt Request Status Flag (IRQF) bit is cleared to 0.
E. Periodic Interrupt Flag (PF) bit is cleared to 0.
F. The device is not accessible until $\overline{\text{RESET}}$ is returned high.
G. Alarm Interrupt Flag (AF) bit is cleared to 0.
H. $\overline{\text{IRQ}}$ pin is in the high impedance state.
I. Square Wave Output Enable ($\overline{\text{SQWE}}$) bit is cleared to 0.
J. Update Ended Interrupt Enable (UIE) is cleared to 0.
K. $\overline{\text{CEO}}$ is driven high.

In a typical application $\overline{\text{RESET}}$ can be connected to V_{CC}. This connection will allow the DS14287 to go in and out of power fail without affecting any of the control registers.

$\overline{\text{CEI}}$ (External RAM Chip Enable Input, active low) - $\overline{\text{CEI}}$ should be driven low to enable the external RAM. $\overline{\text{CEI}}$ is internally pulled up with a 50kΩ resistor.

$\overline{\text{CEO}}$ (External RAM Chip Enable Output, active low) - When V_{CC} is greater than 4.25 volts (typical), $\overline{\text{CEO}}$ will reflect $\overline{\text{CEI}}$ provided the $\overline{\text{RESET}}$ is at a logic high. When V_{CC} is less than 4.25 volts (typical), $\overline{\text{CEO}}$ will be forced to an inactive level regardless of $\overline{\text{CEI}}$.

V_{CCO} (External RAM Power Supply Output) - V_{CCO} provides the higher of V_{CC} or V_{BAT} through an internal switch to power an external RAM.

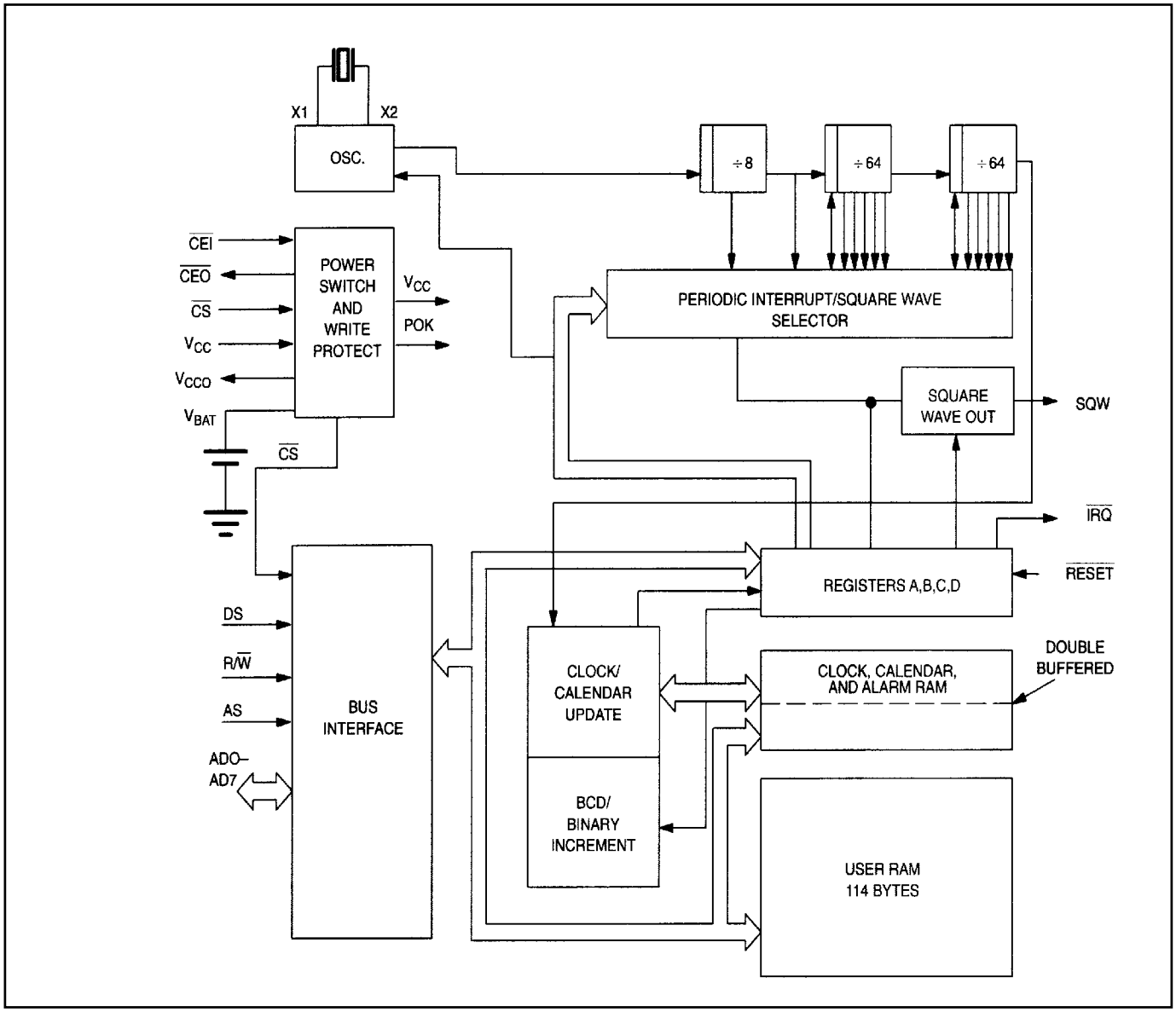
DS14285 Only

X1, X2 - Connections for a standard 32.768 kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks."

V_{BAT} – Battery input for any standard 3-volt lithium cell or other energy source. See the Power-Up/Down section for considerations in selecting the size of the external energy source

The battery should be connected directly to the V_{BAT} pin. A diode must not be placed in series with the battery to the VBAT pin. Furthermore, a diode is not necessary because reverse charging current protection circuitry is provided internal to the device and has passed the requirements of Underwriters Laboratories for UL listing.

Figure 1. DS14285/DS14287 Block Diagram



POWER-DOWN/POWER-UP CONSIDERATIONS

The real time clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS14285/DS14287 and reaches a level of greater than 4.25 volts (typical), the device becomes accessible after 200 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25 volts (typical), the chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin. The DS14285/DS14287 is, therefore, write-protected. When the DS14285/DS14287 is in a write-protected state, all inputs are ignored and all outputs are in a high impedance state. When V_{CC} falls below a level of approximately 3 volts, the external V_{CC} supply is switched off and an internal lithium energy source supplies power to the Real-time Clock and the RAM memory.

An external SRAM can be made nonvolatile by using the V_{CCO} and SRAM chip enable pins (see Figure 1). Nonvolatile control of the external SRAM is analogous to that of the real time clock registers. When V_{CC} slews down during a power fail, $\overline{CEO}$ is driven to an inactive level regardless $\overline{CEI}$. This write protection occurs when V_{CC} is less than 4.25 volts (typical).

During power up, when V_{CC} reaches a level of greater than 4.25 volts (typical), $\overline{CEO}$ will reflect $\overline{CEI}$ after 200 ms. During power-valid operation, the $\overline{CEI}$ input is passed to the $\overline{CEO}$ output with a propagation delay of less than 10 ns.

When V_{CC} is above a level of approximately 3V, the external SRAM will be powered by V_{CC} through the V_{CCO} pin. When V_{CC} is below a level of approximately 3V, the external SRAM will be powered by the internal lithium cell through the V_{CCO} pin. An internal comparator and switch determine whether V_{CCO} is powered by V_{CC} or the internal lithium cell.

When the device is in battery backup mode, the energy source connected to the V_{BAT} pin in the case of the DS14285, or the internal lithium cell in the case of the DS14287 can power an external SRAM for an extended period of time. The amount of time that the lithium cell can supply power to the external SRAM is a function of the data retention current of the SRAM. The capacity of the lithium cell that is encapsulated within the DS14287 module is 130 mAh. If an SRAM with a data retention current of less than 1 μA is used and the oscillator current is 300 nA (typical), the cumulative data retention time is calculated at more than 11 years.

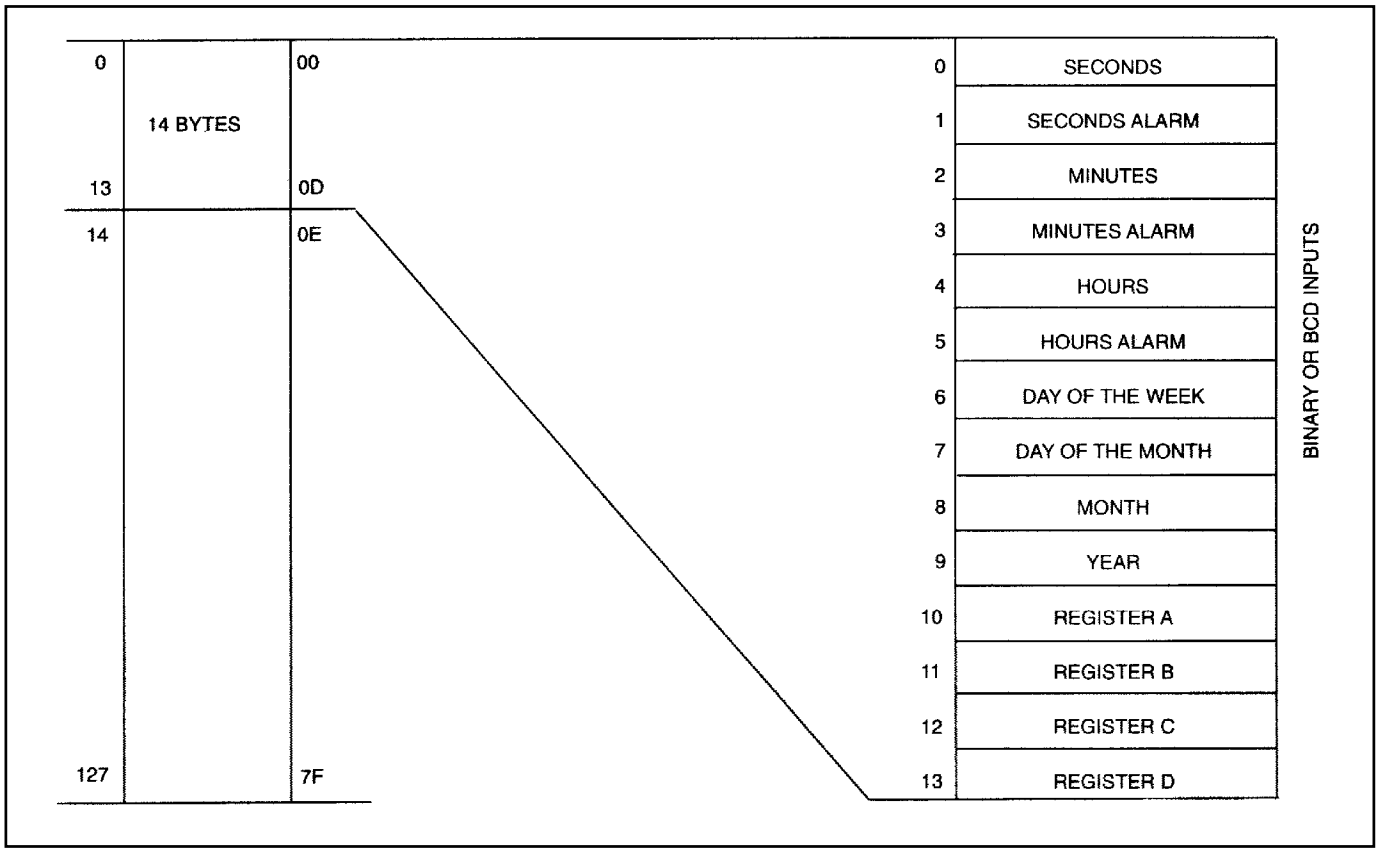
RTC ADDRESS MAP

The address map of the DS14285/DS14287 is shown in Figure 2. The address map consists of 114 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and 4 bytes which are used for control and status. All 128 bytes can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

The contents of four registers (A,B,C, and D) are described in the "Registers" section.

Figure 2. DS14285/DS14287 Address Map



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar, and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the 10 time, calendar, and alarm bytes can be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic 1 to prevent updates from occurring while access is being attempted. In addition to writing the 10 time, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All 10 time, calendar, and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real-time clock to update the time and calendar bytes. Once initialized, the real-time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the 10 data bytes. Table 1 shows the binary and BCD formats of the ten time, calendar, and alarm locations. The

24-12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the 10 bytes are advanced by 1 second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the 3 alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The 2 most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Table 1. Time, Calendar, and Alarm Data Modes

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM, 81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM, 81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

CONTROL REGISTERS

The DS14285/DS14287 has four control registers that are accessible at all times, even during the update cycle.

REGISTER A

MSB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a 1, the update transfer will soon occur. When UIP is a 0, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is 0. The UIP bit is read-only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a 1 inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2 - These 3 bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV0, DV1, and DV2.

RS3, RS2, RS1, RS0 - These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 2 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits. These 4 read/write bits are not affected by $\overline{\text{RESET}}$.

REGISTER B

MSB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET - When the SET bit is a 0, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a 1, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by $\overline{\text{RESET}}$ or internal functions of the DS14285/DS14287.

PIE - The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the $\overline{\text{IRQ}}$ pin low. When the PIE bit is set to 1, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3-RS0 bits of Register A. A 0 in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS14285/DS14287 functions, but is cleared to 0 on $\overline{\text{RESET}}$.

AIE - The Alarm Interrupt Enable (AIE) bit is a read/write bit which, when set to a 1, permits the Alarm Flag (AF) bit in register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the 3 time bytes equal the 3 alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to 0, the AF bit does not initiate the $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AIE to 0. The internal functions of the DS14285/DS14287 do not affect the AIE bit.

UIE - The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears to UIE bit.

SQWE - When the Square Wave Enable (SQWE) bit is set to a 1, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to 0, the SQW pin is held low; the state of SQWE is cleared by the $\overline{\text{RESET}}$ pin. SQWE is a read/write bit.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{\text{RESET}}$. A one in DM signifies binary data while a 0 in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours byte. A 1 indicates the 24-hour mode and a 0 indicates the 12-hour mode. This bit is read/write and is not affected by internal functions of $\overline{\text{RESET}}$.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to 1. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a 0. This bit is not affected by internal functions or $\overline{\text{RESET}}$.

REGISTER C

MSB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF - The Interrupt Request Flag (IRQF) bit is set to a 1 when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

That is, IRQF = PF • PIE + AF • AIE + UF • UIE.

Any time the IRQF bit is a 1, the $\overline{\text{IRQ}}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{\text{RESET}}$ pin is low.

PF - The Periodic Interrupt Flag (PF) is a read-only bit which is set to a 1 when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a 1 independent of the state of the PIE bit. When both PF and PIE are 1s, the $\overline{\text{IRQ}}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{\text{RESET}}$ or a software read of Register C.

AF - A 1 in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a 1, the $\overline{\text{IRQ}}$ pin will go low and a one will appear in the IRQF bit. A $\overline{\text{RESET}}$ or a read of Register C will clear AF.

UF - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to 1, the 1 in UF causes the IRQF bit to be a 1 which will assert the $\overline{\text{IRQ}}$ pin. UF is cleared by reading Register C or a $\overline{\text{RESET}}$.

BIT 0 THROUGH BIT 3 - These are unused bits of the status Register C. These bits always read 0 and cannot be written.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit indicates the condition of the internal battery (the battery connected to the V_{BAT} pin in the case of the DS14285S, DS14285, and the DS14285Q). This bit is not writable and should always be a 1 when read. If a 0 is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{\text{RESET}}$.

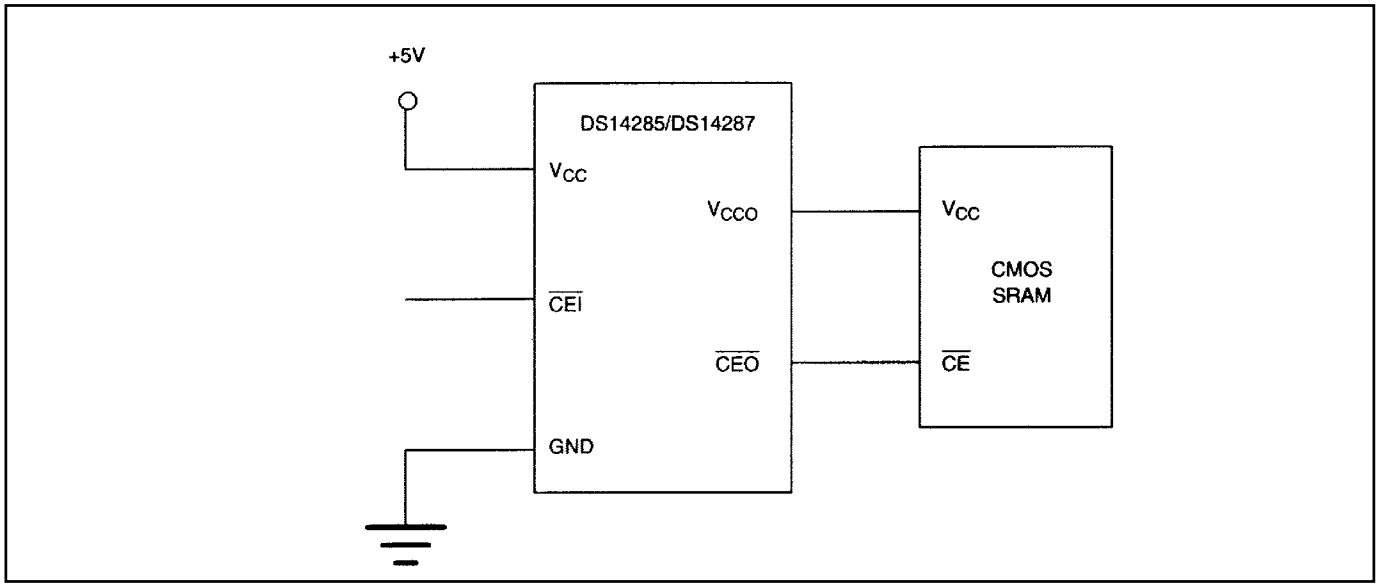
BIT 6 THROUGH BIT 0 - The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read 0.

NONVOLATILE RAM

The 114 general-purpose nonvolatile RAM bytes are not dedicated to any special function within the DS14285/DS14287. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

The DS14285/DS14287 can also provide additional nonvolatile RAM. This is accomplished through the use of its internal lithium cell in the case of the DS14287 (or the energy source connected to the V_{BAT} pin in the case of the DS14285) and battery-backup controller to make a standard CMOS SRAM nonvolatile during power-fail conditions. During power-fail, the DS14285/DS14287 automatically write-protects the external SRAM and provides a V_{CC} output sourced from the internal lithium cell. The interface between the DS14285/DS14287 and an external SRAM is illustrated in Figure 3.

Figure 3. External SRAM Interface to the DS14285/DS14287 RTC



INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A 0 in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts. When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the

flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, 2, or 3 bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS14285/DS14287. The act of reading Register C clears all active flag bits and the IRQF bit.

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 2). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

OSCILLATOR CONTROL BITS

When the DS14287 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE-WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 2. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

Table 2. Periodic Interrupt Rate and Square-Wave Output Frequency

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625ms	256Hz
0	0	1	0	7.8125ms	128Hz
0	0	1	1	122.070µs	8.192kHz
0	1	0	0	244.141µs	4.096kHz
0	1	0	1	488.281µs	2.048kHz
0	1	1	0	976.5625µs	1.024kHz
0	1	1	1	1.953125ms	512Hz
1	0	0	0	3.90625ms	256Hz
1	0	0	1	7.8125ms	128Hz
1	0	1	0	15.625ms	64Hz
1	0	1	1	31.25ms	32Hz
1	1	0	0	62.5ms	16Hz
1	1	0	1	125ms	8Hz
1	1	1	0	250ms	4Hz
1	1	1	1	500ms	2Hz

UPDATE CYCLE

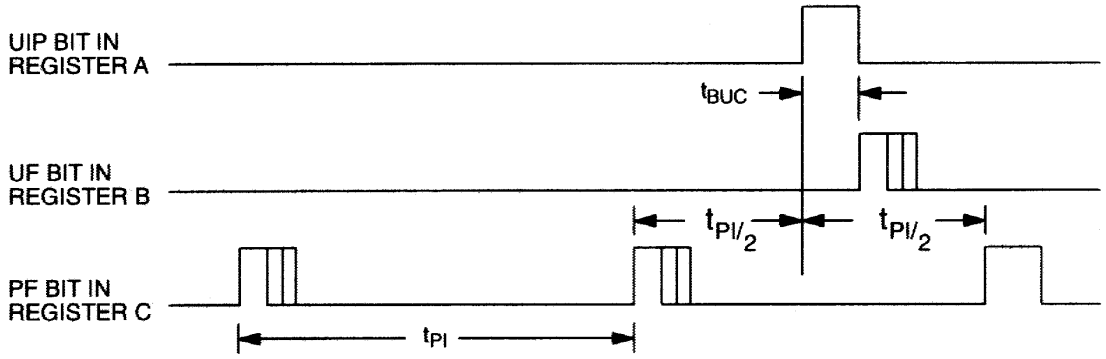
The DS14285/DS14287 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a “don’t care” code is present in all three positions.

There are three methods that can handle access of the real-time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every up date cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 4). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within 1 ($t_{PI/2}$ + t_{BUC}) to ensure that data is not read during the update cycle.

Figure 4. Update-Ended and Periodic Interrupt Relationship



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 µs.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.5V to +7.0V
Storage Temperature Range……...-40°C to +85°C
Soldering Temperature: DIP……..260°C for 10 seconds (See Note 12)
Soldering Temperature: Surface Mount:…….See IPC/JEDEC Standard J-STD-020

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial	-40°C to +85°C	5V ±10%

RECOMMENDED DC OPERATING CONDITIONS

(Over the operating range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power-Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Battery Voltage	V_{BAT}	2.5		3.6	V	1
Input Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(Over the operating range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		7	15	mA	2
Oscillator Current	I_{OSC}		300	500	nA	
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
I/O Leakage	I_{LO}	-1.0		+1.0	µA	5
MOT Input Current	I_{MOT}	-1.0		+500	µA	3
$\overline{CEI}$ Input Current	$I_{\overline{CEI}}$	-1.0		+200	µA	4
$\overline{CEI}$ to $\overline{CEO}$ Impedance	Z_{CE}			60	Ω	11
Output at 2.4V	I_{OH}	-1.0			mA	1, 6
Output at 0.4V	I_{OL}			4.0	mA	1
Write-Protect Voltage	V_{TP}	4.0	4.25	4.5	V	
V_{CCO} Voltage	V_{CCO1}	V_{CC} - 0.3V			V	7
	V_{CCO2}	V_{BAT} - 0.3V				8

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

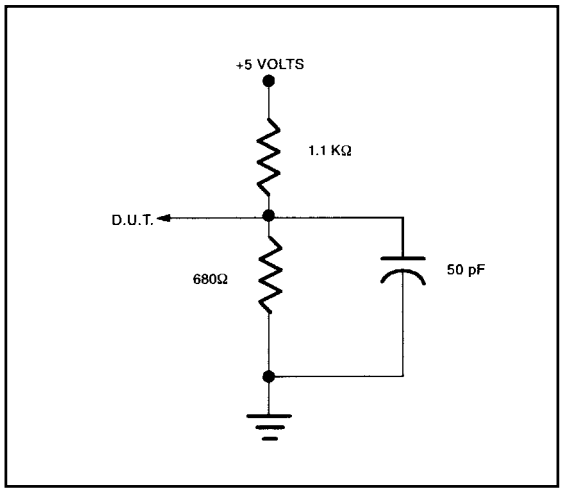
(Over the operating range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle	t_{CYC}	225		DC	ns	
Pulse Width, DS/E Low or RD/$\overline{WR}$ High	PW_{EL}	115			ns	
Pulse Width, DS/E Low or RD/$\overline{WR}$ Low	PW_{EH}	80			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}	10			ns	
Chip Select Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS/E to AS/ALE Rise	t_{ASD}	20			ns	
Pulse Width AS/ALE High	PW_{ASH}	60			ns	
Delay Time, AS/ALE to DS/E Rise	t_{ASED}	35			ns	
Output Data Delay Time From DS/E or $\overline{RD}$	t_{DDR}	10		75	ns	9
Data Setup Time	t_{DSW}	60			ns	
Reset Pulse Width	t_{RWL}	5			µs	
$\overline{IRQ}$ Release from DS	t_{IRDS}			2	µs	
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}			2	µs	

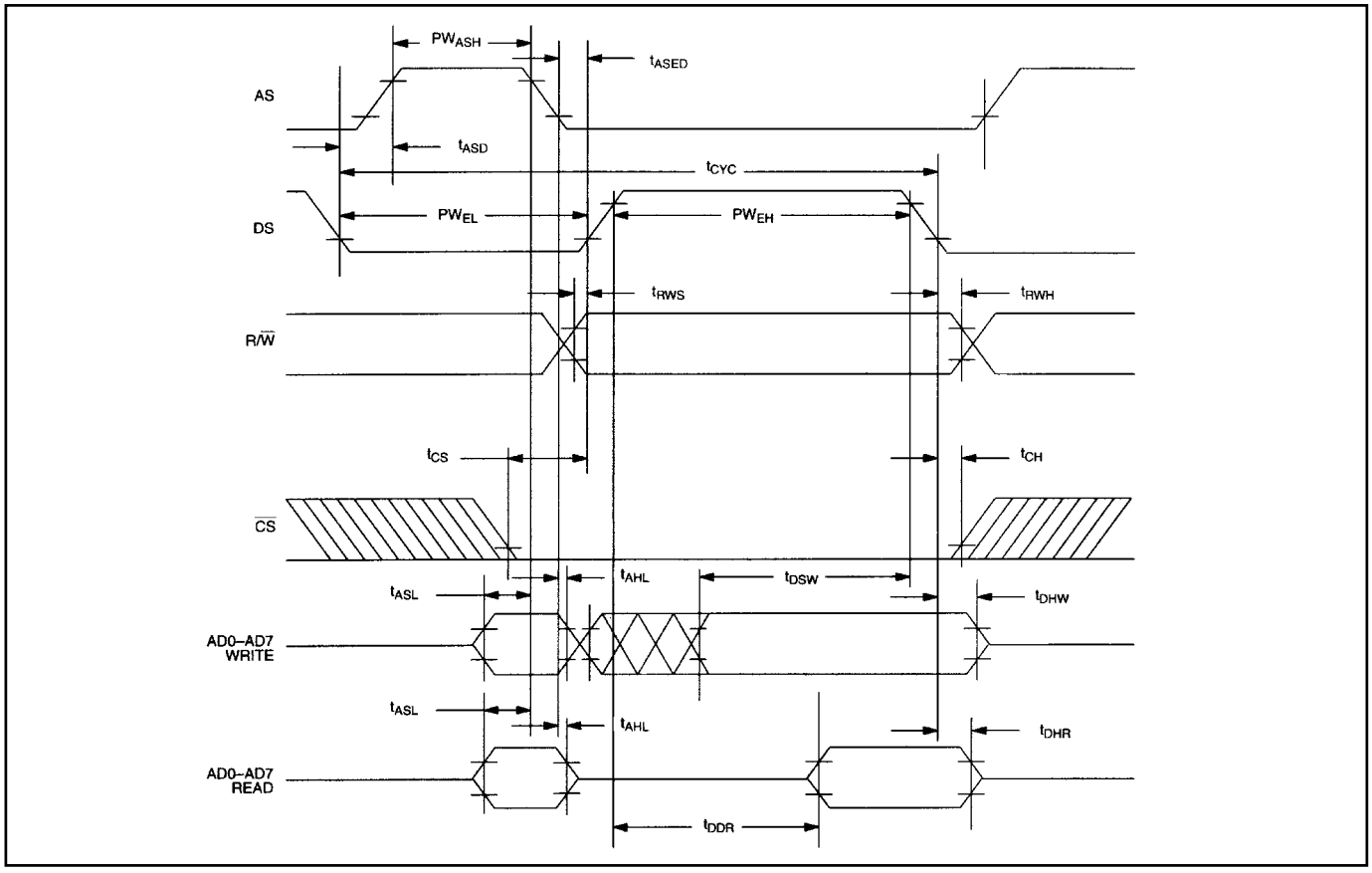
AC TEST CONDITIONS

Input Pulse Level: 0 to 3.0V
Input Rise/Fall Times: 5ns
Input and Output Timing Reference Levels: 1.5V

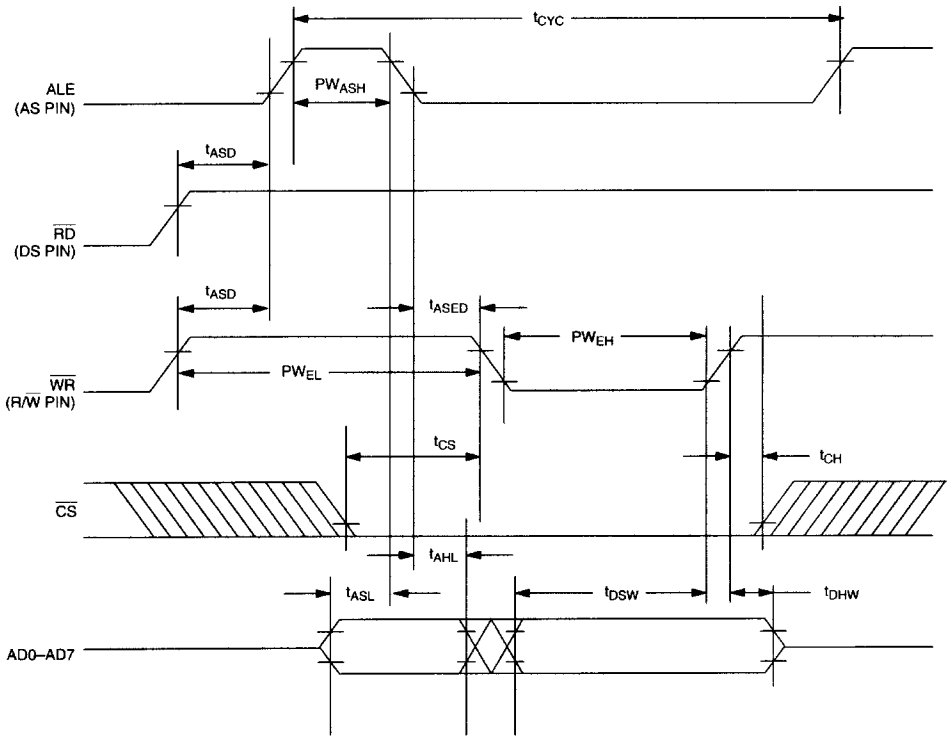
Figure 5. Output Load



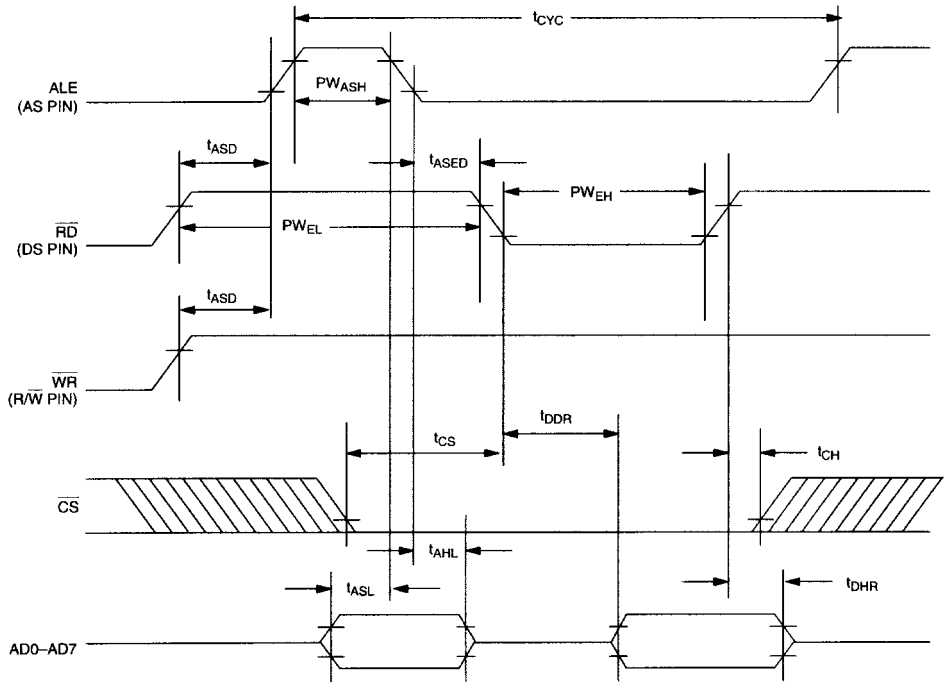
DS14285 BUS TIMING FOR MOTOROLA INTERFACE



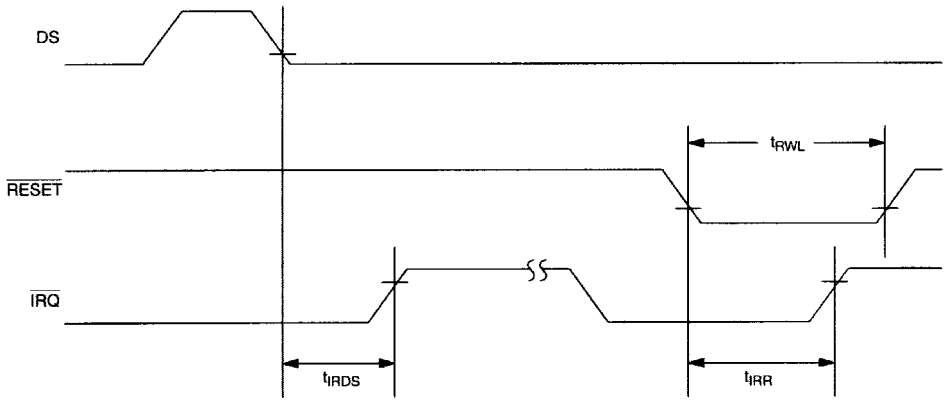
DS14285/DS14287 BUS TIMING FOR INTEL INTERFACE WRITE CYCLE



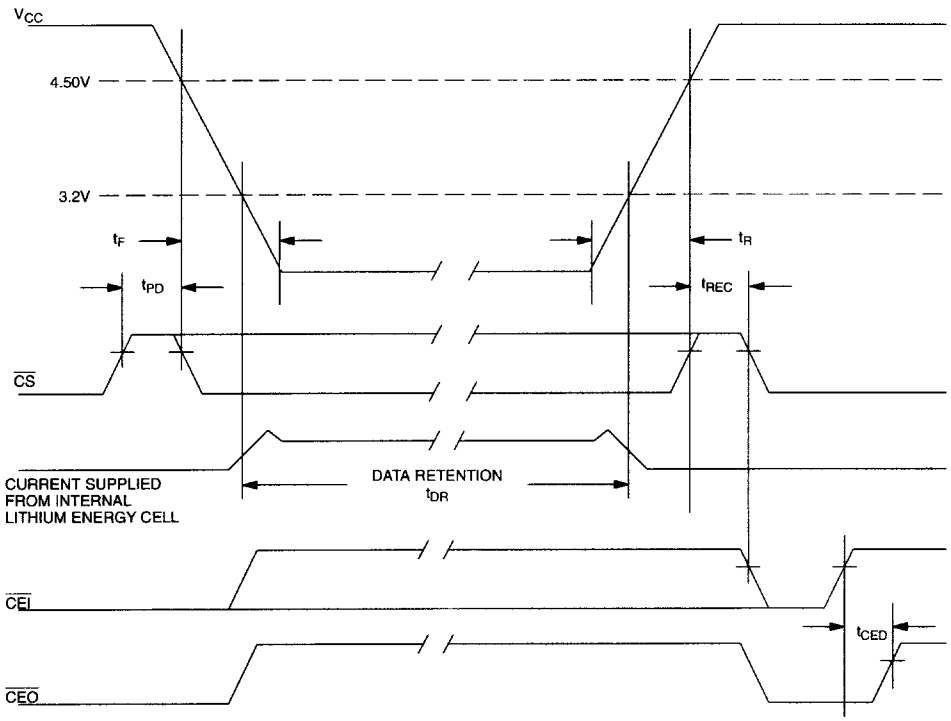
DS14285/DS14287 BUS TIMING FOR INTEL INTERFACE READ CYCLE



DS14285/DS14287 IRQ RELEASE DELAY TIMING



POWER-DOWN/POWER-UP TIMING



POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} slew from 4.5V to 0V ($\overline{CS}$ at V_{IH})	t_F	300			µs	
V_{CC} slew from 0V to 4.5V ($\overline{CS}$ at V_{IH})	t_R	100			µs	
$\overline{CS}$ at V_{IH} after Power-Up	t_{REC}	20		200	ms	
Chip-Enable Propagation Delay to External SRAM	t_{CED}			10	ns	

(T_A = +25°C)

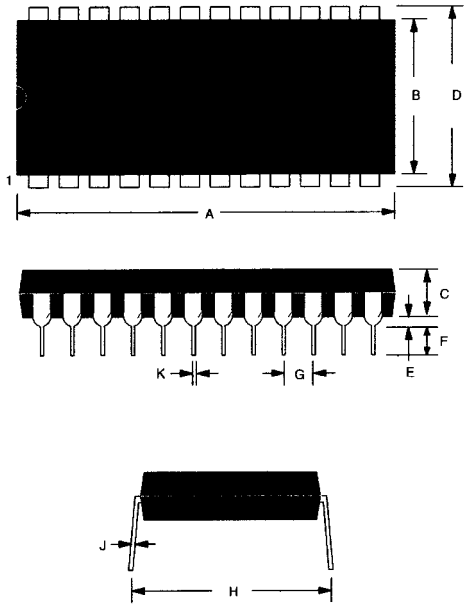
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention for DS14287	t_{DR}	10			years	10

NOTE: The RTC keeps time to an accuracy of +1 minute per month during data retention time for the period of t_{DR}.

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

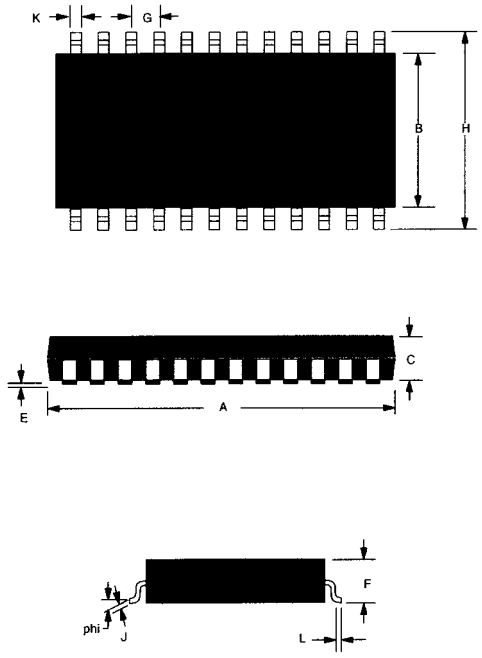
NOTES:

1) All voltages are referenced to ground.
2) All outputs are open.
3) The MOT pin has an internal pulldown of 20kΩ.
4) The $\overline{CEI}$ pin has an internal pullup of 50kΩ.
5) Applies to the AD0–AD7 pins, the $\overline{IRQ}$ pin, and the SQW pin when each is in the high impedance state.
6) The $\overline{IRQ}$ pin is open drain. The interrupt and the internal clock continue to run regardless of the level of VCC. However, it is important to insure that the pullup resistor used with the interrupt pin is never pulled up to a value which is greater than V_{CC} + 0.3V. As VCC falls below approximately 3.0 volts, a power switching circuit turns the lithium energy source on to maintain the clock and timer data functionality.
7) I_{CCO} = 100mA, $V_{CC} > V_{BAT}$.
8) I_{CCO} = 100µA, $V_{CC} < V_{BAT}$.
9) Measured with a load as shown in Figure 5.
10) Expected data retention is based on using an external SRAM with a data retention current of less than 1µA at +25°C.
11) Z_{CE} is an average input-to-output impedance as the input is swept from ground to V_{CCI} and less than 4mA is forced through Z_{CE}.
12) Real-Time Clock Modules such as the DS14287 can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used.



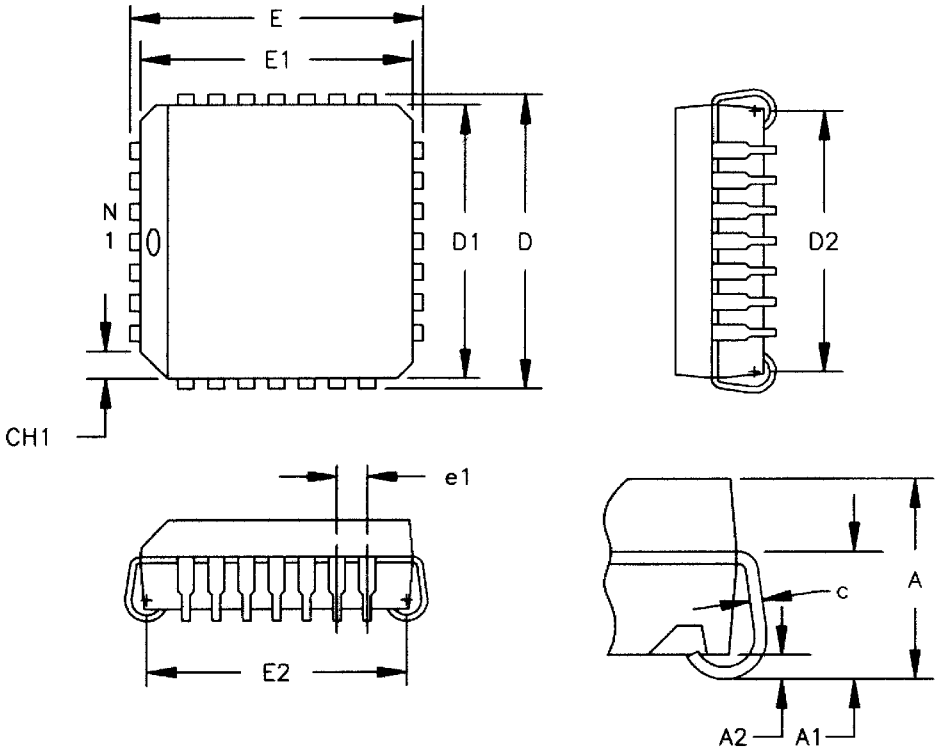
PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.245	1.270
MM	31.62	32.25
B IN.	0.530	0.550
MM	13.46	13.97
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.600	0.625
MM	15.24	15.88
E IN.	0.015	0.050
MM	0.380	1.27
F IN.	0.120	0.145
MM	3.05	3.68
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.022
MM	0.38	0.56

DS14285 24-PIN SO



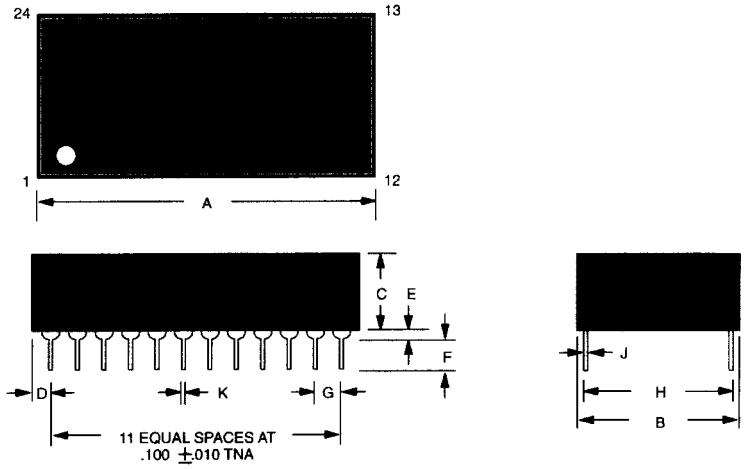
PKG	24-PIN	
DIM	MIN	MAX
A IN.	0.602	0.612
MM	15.29	15.54
B IN.	0.290	0.300
MM	7.37	7.65
C IN.	0.089	0.095
MM	2.26	2.41
E IN.	0.004	0.012
MM	0.102	0.30
F IN.	0.094	0.105
MM	2.38	2.68
G IN.	0.050 BSC	
MM	1.27 BSC	
H IN.	0.398	0.416
MM	10.11	10.57
J IN.	0.009	0.013
MM	0.229	0.33
K IN.	0.013	0.019
MM	0.33	0.48
L IN.	0.016	0.040
MM	0.406	1.02
phi	0°	8°

DS14285Q 28-PIN PLCC



PKG	28-PIN	
DIM	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	-
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
D	0.485	0.495
D1	0.450	0.456
D2	0.390	0.430
E	0.485	0.495
E1	0.450	0.456
E2	0.390	0.430
L1	0.060	-
N	28	-
e1	0.050 BSC	
CH1	0.042	0.048

DS14287 REAL-TIME CLOCK PLUS RAM



PKG	24-PIN	
DIM	MIN	MAX
A IN.	1.320	1.335
MM	33.53	33.91
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.345	0.370
MM	8.76	9.40
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

NOTE: PINS 2, 3, 16, AND 20 ARE MISSING BY DESIGN.