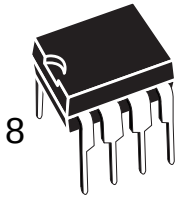
M93C86, M93C76, M93C66
M93C56, M93C46, M93C06

16Kbit, 8Kbit, 4Kbit, 2Kbit, 1Kbit and 256bit (8-bit or 16-bit wide) MICROWIRE Serial Access EEPROM

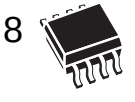
FEATURES SUMMARY

- Industry Standard MICROWIRE Bus
- Single Supply Voltage:
  - 4.5V to 5.5V for M93Cx6
  - 2.5V to 5.5V for M93Cx6-W
  - 1.8V to 5.5V for M93Cx6-R
- Dual Organization: by Word (x16) or Byte (x8)
- Programming Instructions that work on: Byte, Word or Entire Memory
- Self-timed Programming Cycle with Auto-Erase
- Ready/$\overline{\text{Busy}}$ Signal During Programming
- Speed:
  - 1MHz Clock Rate, 10ms Write Time (Current product, identified by process identification letter F or M)
  - 2MHz Clock Rate, 5ms Write Time (New Product, identified by process identification letter W)
- Sequential Read Operation
- Enhanced ESD/Latch-Up Behaviour
- More than 1 Million Erase/Write Cycles
- More than 40 Year Data Retention

Figure 1. Packages



PDIP8 (BN)



SO8 (MN)
150 mil width



TSSOP8 (DS)
3x3mm body size



TSSOP8 (DW)
169 mil width

M93C06 IS “NOT FOR NEW DESIGN”

The M93C06 is still in production, but is not recommended for new designs. Please refer to AN1571 on how to replace the M93C06 by the M93C46 in your application.

SUMMARY DESCRIPTION

These electrically erasable programmable memory (EEPROM) devices are accessed through a Serial Data Input (D) and Serial Data Output (Q) using the MICROWIRE bus protocol.

Figure 2. Logic Diagram

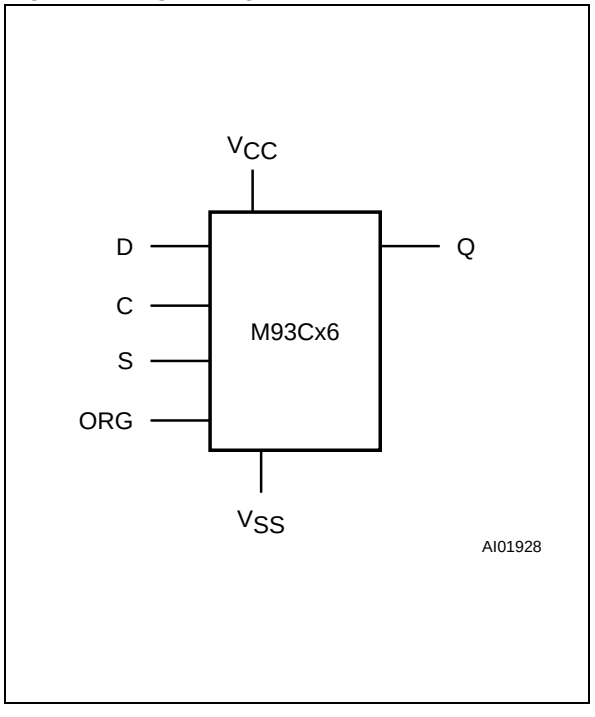


Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

The memory array organization may be divided into either bytes (x8) or words (x16) which may be selected by a signal applied on Organization Select (ORG). The bit, byte and word sizes of the memories are as shown in Table 2.

Table 2. Memory Size versus Organization

Device	Number of Bits	Number of 8-bit Bytes	Number of 16-bit Words
M93C86	16384	2048	1024
M93C76	8192	1024	512
M93C66	4096	512	256
M93C56	2048	256	128
M93C46	1024	128	64
M93C06[1]	256	32	16

Note: 1. Not for New Design

The M93Cx6 is accessed by a set of instructions, as summarized in Table 3, and in more detail in Table 4 to Table 6).

Table 3. Instruction Set for the M93Cx6

Instruction	Description	Data
READ	Read Data from Memory	Byte or Word
WRITE	Write Data to Memory	Byte or Word
EWEN	Erase/Write Enable	
EWDS	Erase/Write Disable	
ERASE	Erase Byte or Word	Byte or Word
ERAL	Erase All Memory	
WRAL	Write All Memory with same Data	

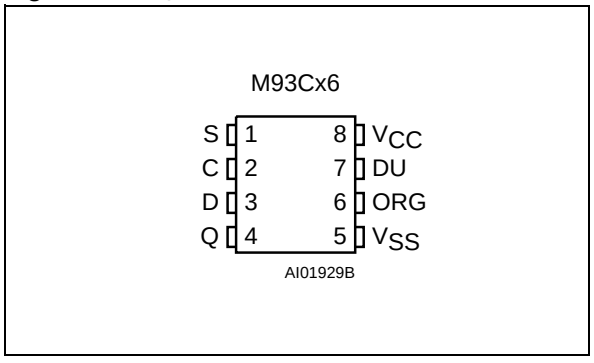
A Read Data from Memory (READ) instruction loads the address of the first byte or word to be read in an internal address register. The data at this address is then clocked out serially. The address register is automatically incremented after the data is output and, if Chip Select Input (S) is held High, the M93Cx6 can output a sequential stream of data bytes or words. In this way, the memory can be read as a data stream from eight to 16384 bits long (in the case of the M93C86), or continuously (the address counter automatically rolls over to 00h when the highest address is reached).

Programming is internally self-timed (the external clock signal on Serial Clock (C) may be stopped or left running after the start of a Write cycle) and does not require an Erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at a time into one of the byte or word locations of the M93Cx6. After the start of the programming cy-

cle, a Busy/Ready signal is available on Serial Data Output (Q) when Chip Select Input (S) is driven High.

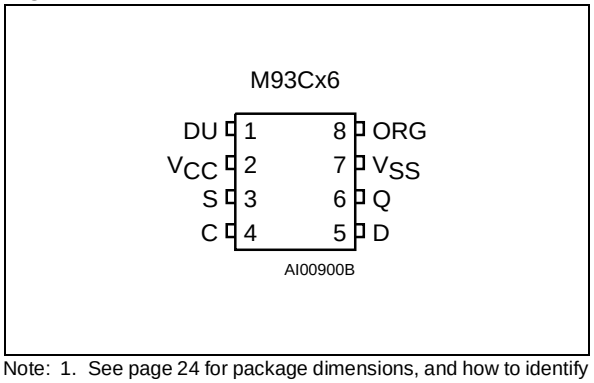
An internal Power-on Data Protection mechanism in the M93Cx6 inhibits the device when the supply is too low.

Figure 3. DIP, SO and TSSOP Connections



Note: 1. See page 21 (onwards) for package dimensions, and how to identify pin-1.
2. DU = Don't Use.

Figure 4. 90° Turned-SO Connections



Note: 1. See page 24 for package dimensions, and how to identify pin-1.
2. DU = Don't Use.

The DU (Don't Use) pin does not contribute to the normal operation of the device. It is reserved for use by STMicroelectronics during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest stand-by power consumption.

MEMORY ORGANIZATION

The M93Cx6 memory is organized either as bytes (x8) or as words (x16). If Organization Select (ORG) is left unconnected (or connected to V_{CC}) the x16 organization is selected; when Organization Select (ORG) is connected to Ground (V_{SS}) the x8 organization is selected. When the M93Cx6 is in stand-by mode, Organization Select (ORG) should be set either to V_{SS} or V_{CC} for minimum power consumption. Any voltage between V_{SS} and V_{CC} applied to Organization Select (ORG) may increase the stand-by current.

POWER-ON DATA PROTECTION

To prevent data corruption and inadvertent write operations during power-up, a Power-On Reset (POR) circuit resets all internal programming circuitry, and sets the device in the Write Disable mode.

– At Power-up and Power-down, the device must *not* be selected (that is, Chip Select Input (S) must be driven Low) until the supply voltage reaches the operating value V_{CC} specified in Table 8 to Table 10.

– When V_{CC} reaches its valid level, the device is properly reset (in the Write Disable mode) and is ready to decode and execute incoming instructions.

For the M93Cx6 devices (5V range) the POR threshold voltage is around 3V. For the M93Cx6-W (3V range) and M93Cx6-R (2V range) the POR threshold voltage is around 1.5V.

INSTRUCTIONS

The instruction set of the M93Cx6 devices contains seven instructions, as summarized in Table 4 to Table 6. Each instruction consists of the following parts, as shown in Figure 5:

- Each instruction is preceded by a rising edge on Chip Select Input (S) with Serial Clock (C) being held Low.
- A start bit, which is the first '1' read on Serial Data Input (D) during the rising edge of Serial Clock (C).
- Two op-code bits, read on Serial Data Input (D) during the rising edge of Serial Clock (C). (Some instructions also use the first two bits of the address to define the op-code).
- The address bits of the byte or word that is to be accessed. For the M93C46, the address is made up of 6 bits for the x16 organization or 7 bits for the x8 organization (see Table 4). For the M93C56 and M93C66, the address is made up of 8 bits for the x16 organization or 9 bits for the x8 organization (see Table 5). For the M93C76 and M93C86, the address is made up of 10 bits for the x16 organization or 11 bits for the x8 organization (see Table 6).

The M93Cx6 devices are fabricated in CMOS technology and are therefore able to run as slow as 0 Hz (static input signals) or as fast as the maximum ratings specified in Table 19 to Table 22.

Table 4. Instruction Set for the M93C46 and M93C06

Instruction	Description	Start bit	Op-Code	x8 Origination (ORG = 0)			x16 Origination (ORG = 1)		
				Address[1,2]	Data	Required Clock Cycles	Address[1,3]	Data	Required Clock Cycles
READ	Read Data from Memory	1	10	A6-A0	Q7-Q0		A5-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A6-A0	D7-D0	18	A5-A0	D15-D0	25
EWEN	Erase/Write Enable	1	00	11X XXXX		10	11 XXXX		9
EWDS	Erase/Write Disable	1	00	00X XXXX		10	00 XXXX		9
ERASE	Erase Byte or Word	1	11	A6-A0		10	A5-A0		9
ERAL	Erase All Memory	1	00	10X XXXX		10	10 XXXX		9
WRAL	Write All Memory with same Data	1	00	01X XXXX	D7-D0	18	01 XXXX	D15-D0	25

Note: 1. X = Don't Care bit.
2. Address bits A6 and A5 are not decoded by the M93C06.
3. Address bits A5 and A4 are not decoded by the M93C06.

Table 5. Instruction Set for the M93C56 and M93C66

Instruction	Description	Start bit	Op-Code	x8 Origination (ORG = 0)			x16 Origination (ORG = 1)		
				Address[1,2]	Data	Required Clock Cycles	Address[1,3]	Data	Required Clock Cycles
READ	Read Data from Memory	1	10	A8-A0	Q7-Q0		A7-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A8-A0	D7-D0	20	A7-A0	D15-D0	27
EWEN	Erase/Write Enable	1	00	1 1XXX XXXX		12	11XX XXXX		11
EWDS	Erase/Write Disable	1	00	0 0XXX XXXX		12	00XX XXXX		11
ERASE	Erase Byte or Word	1	11	A8-A0		12	A7-A0		11
ERAL	Erase All Memory	1	00	1 0XXX XXXX		12	10XX XXXX		11
WRAL	Write All Memory with same Data	1	00	0 1XXX XXXX	D7-D0	20	01XX XXXX	D15-D0	27

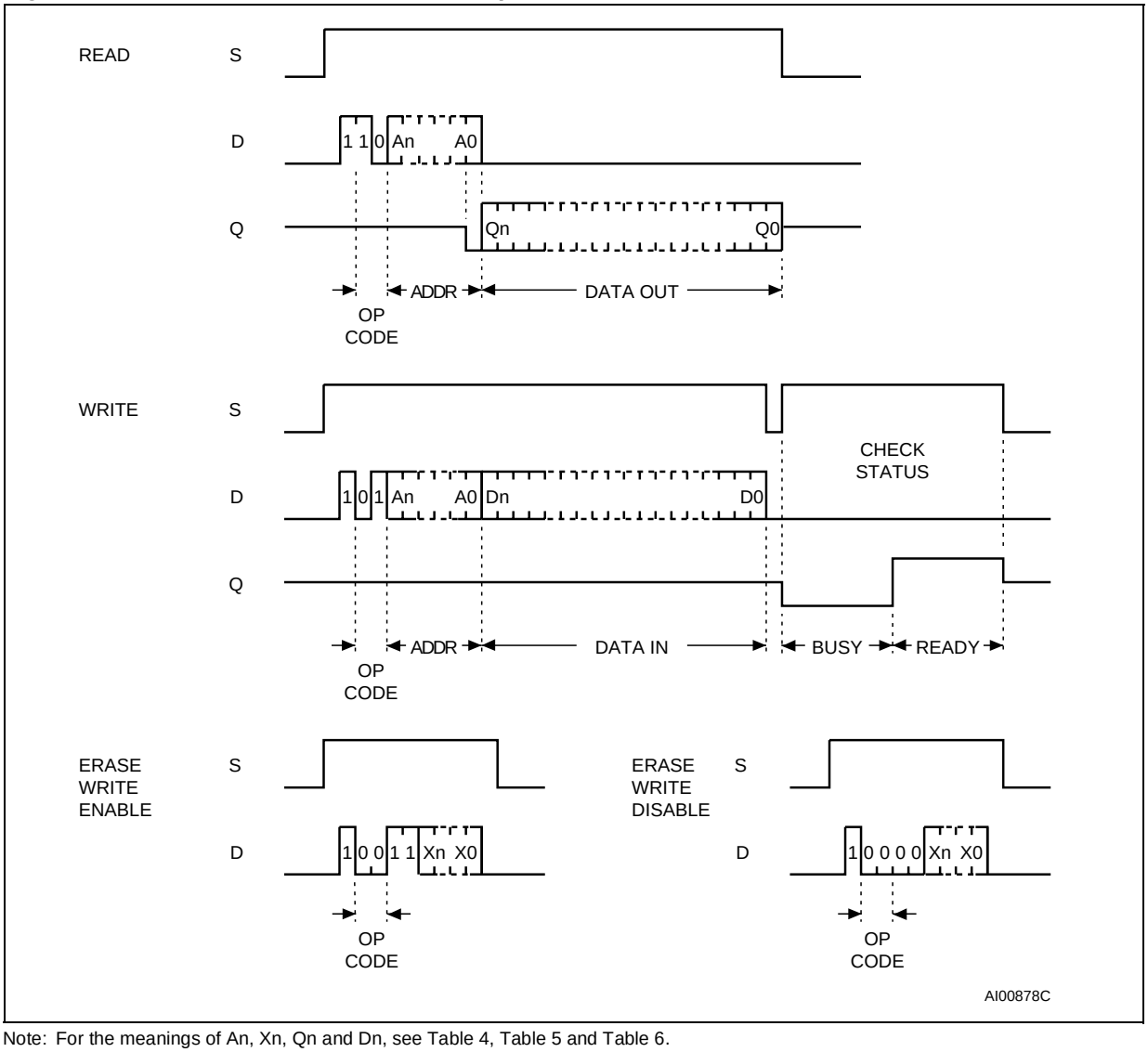
Note: 1. X = Don't Care bit.
2. Address bit A8 is not decoded by the M93C56.
3. Address bit A7 is not decoded by the M93C56.

Table 6. Instruction Set for the M93C76 and M93C86

Instruction	Description	Start bit	Op-Code	x8 Origination (ORG = 0)			x16 Origination (ORG = 1)		
				Address[1,2]	Data	Required Clock Cycles	Address[1,3]	Data	Required Clock Cycles
READ	Read Data from Memory	1	10	A10-A0	Q7-Q0		A9-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A10-A0	D7-D0	22	A9-A0	D15-D0	29
EWEN	Erase/Write Enable	1	00	11X XXXX XXXX		14	11 XXXX XXXX		13
EWDS	Erase/Write Disable	1	00	00X XXXX XXXX		14	00 XXXX XXXX		13
ERASE	Erase Byte or Word	1	11	A10-A0		14	A9-A0		13
ERAL	Erase All Memory	1	00	10X XXXX XXXX		14	10 XXXX XXXX		13
WRAL	Write All Memory with same Data	1	00	01X XXXX XXXX	D7-D0	22	01 XXXX XXXX	D15-D0	29

Note: 1. X = Don't Care bit.
2. Address bit A10 is not decoded by the M93C76.
3. Address bit A9 is not decoded by the M93C76.

Figure 5. READ, WRITE, EWEN, EWDS Sequences



Note: For the meanings of An, Xn, Qn and Dn, see Table 4, Table 5 and Table 6.

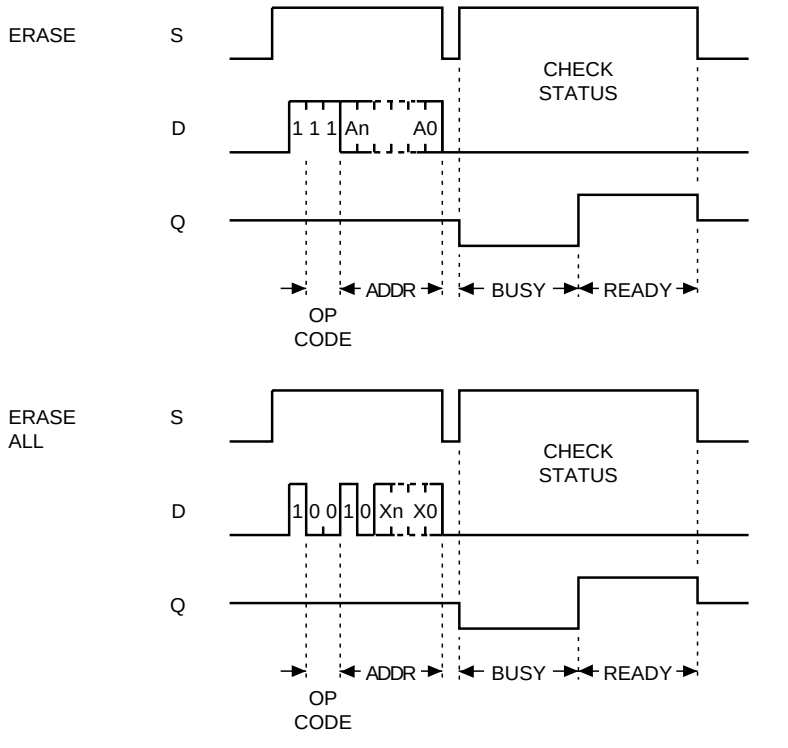
Read

The Read Data from Memory (READ) instruction outputs serial data on Serial Data Output (Q). When the instruction is received, the op-code and address are decoded, and the data from the memory is transferred to an output shift register. A dummy 0 bit is output first, followed by the 8-bit byte or the 16-bit word, with the most significant bit first. Output data changes are triggered by the rising edge of Serial Clock (C). The M93Cx6 automatically increments the internal address register and clocks out the next byte (or word) as long as the Chip Select Input (S) is held High. In this case, the dummy 0 bit is *not* output between bytes (or words) and a continuous stream of data can be read.

Erase/Write Enable and Disable

The Erase/Write Enable (EWEN) instruction enables the future execution of erase or write instructions, and the Erase/Write Disable (EWDS) instruction disables it. When power is first applied, the M93Cx6 initializes itself so that erase and write instructions are disabled. After an Erase/Write Enable (EWEN) instruction has been executed, erasing and writing remains enabled until an Erase/Write Disable (EWDS) instruction is executed, or until V_{CC} falls below the power-on reset threshold voltage. To protect the memory contents from accidental corruption, it is advisable to issue the Erase/Write Disable (EWDS) instruction after every write cycle. The Read Data from Memory (READ) instruction is not affected by the Erase/Write Enable (EWEN) or Erase/Write Disable (EWDS) instructions.

Figure 6. ERASE, ERAL Sequences



Note: For the meanings of An and Xn, please see Table 4, Table 5 and Table 6.

Erase

The Erase Byte or Word (ERASE) instruction sets the bits of the addressed memory byte (or word) to 1. Once the address has been correctly decoded, the falling edge of the Chip Select Input (S) starts the self-timed Erase cycle. The completion of the cycle can be detected by monitoring the Ready/Busy line, as described on page 7.

Write

For the Write Data to Memory (WRITE) instruction, 8 or 16 data bits follow the op-code and address bits. These form the byte or word that is to be written. As with the other bits, Serial Data Input (D) is sampled on the rising edge of Serial Clock (C).

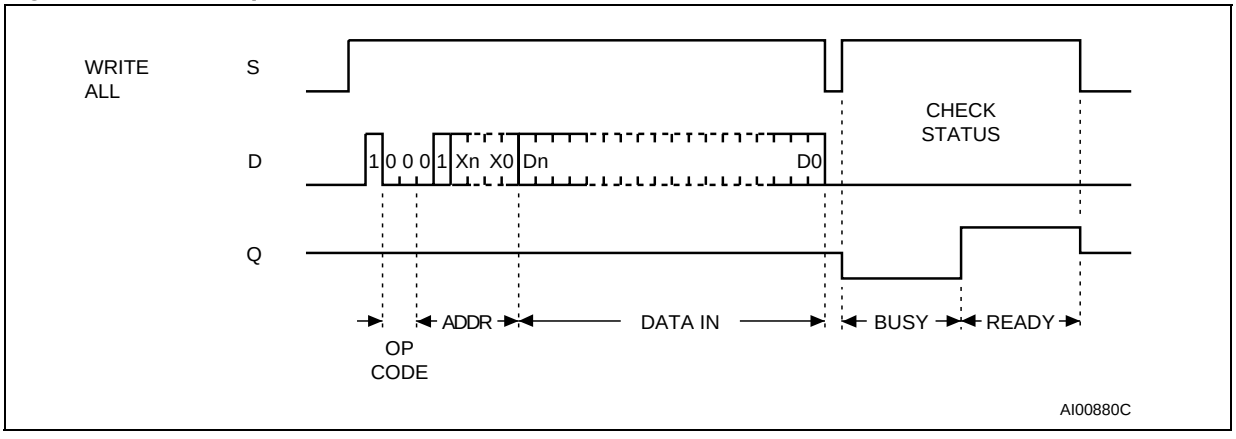
After the last data bit has been sampled, *the Chip Select Input (S) must be taken Low before the next rising edge of Serial Clock (C).* If Chip Select Input (S) is brought Low before or after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed. The completion of the cycle can be detected by monitoring the Ready/Busy line, as described later in this document.

Once the Write cycle has been started, it is internally self-timed (the external clock signal on Serial Clock (C) may be stopped or left running after the start of a Write cycle). The cycle is automatically preceded by an Erase cycle, so it is unnecessary to execute an explicit erase instruction before a Write Data to Memory (WRITE) instruction.

Erase All

The Erase All Memory (ERAL) instruction erases the whole memory (all memory bits are set to 1). The format of the instruction requires that a dummy address be provided. The Erase cycle is conducted in the same way as the Erase instruction (ERASE). The completion of the cycle can be detected by monitoring the Ready/Busy line, as described on page 7.

Figure 7. WRAL Sequence



Note: For the meanings of Xn and Dn, please see Table 4, Table 5 and Table 6.

Write All

As with the Erase All Memory (ERAL) instruction, the format of the Write All Memory with same Data (WRAL) instruction requires that a dummy address be provided. As with the Write Data to Memory (WRITE) instruction, the format of the Write All Memory with same Data (WRAL) instruction requires that an 8-bit data byte, or 16-bit data word, be provided. This value is written to all the addresses of the memory device. The completion of the cycle can be detected by monitoring the Ready/$\overline{\text{Busy}}$ line, as described next.

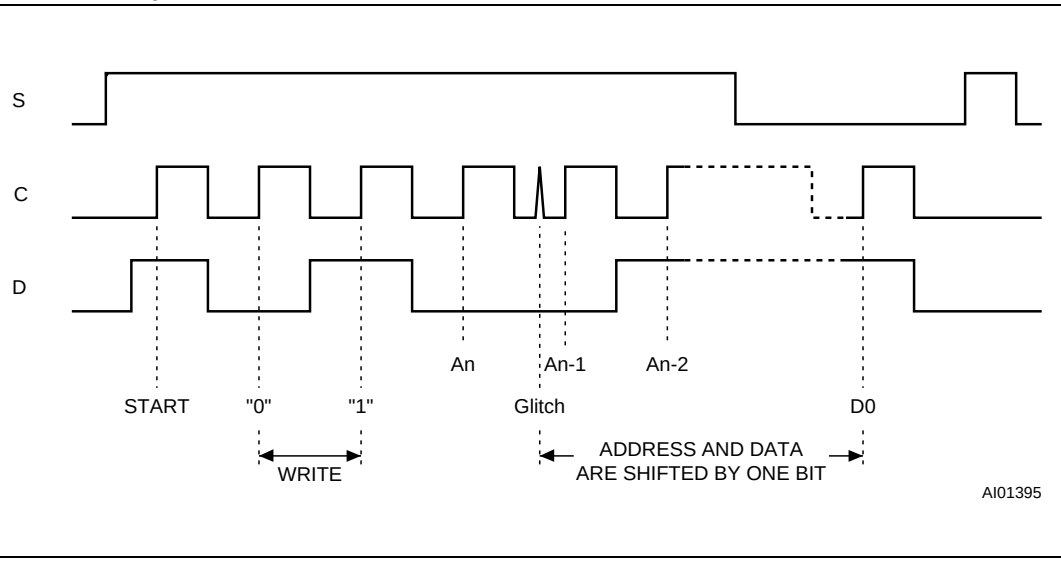
READY/$\overline{\text{BUSY}}$ STATUS

While the Write or Erase cycle is underway, for a WRITE, ERASE, WRAL or ERAL instruction, the Busy signal (Q=0) is returned whenever Chip Select Input (S) is driven High. (Please note, though, that there is an initial delay, of t_{SLSH}, before this status information becomes available). In this state, the M93Cx6 ignores any data on the bus. When the Write cycle is completed, and Chip Select Input (S) is driven High, the Ready signal (Q=1) indicates that the M93Cx6 is ready to receive the next instruction. Serial Data Output (Q) remains set to 1 until the Chip Select Input (S) is brought Low or until a new start bit is decoded.

COMMON I/O OPERATION

Serial Data Output (Q) and Serial Data Input (D) can be connected together, through a current limiting resistor, to form a common, single-wire data bus. Some precautions must be taken when operating the memory in this way, mostly to prevent a short circuit current from flowing when the last address bit (A0) clashes with the first data bit on Serial Data Output (Q). Please see the application note *AN394* for details.

Figure 8. Write Sequence with One Clock Glitch



CLOCK PULSE COUNTER

In a noisy environment, the number of pulses received on Serial Clock (C) may be greater than the number delivered by the master (the microcontroller). This can lead to a misalignment of the instruction of one or more bits (as shown in Figure 8) and may lead to the writing of erroneous data at an erroneous address.

To combat this problem, the M93Cx6 has an on-chip counter that counts the clock pulses from the start bit until the falling edge of the Chip Select Input (S). If the number of clock pulses received is not the number expected, the WRITE, ERASE, ERAL or WRAL instruction is aborted, and the contents of the memory are not modified.

The number of clock cycles expected for each instruction, and for each member of the M93Cx6 family, are summarized in Table 4 to Table 6. For example, a Write Data to Memory (WRITE) instruction on the M93C56 (or M93C66) expects 20 clock cycles (for the x8 organization) from the start bit to the falling edge of Chip Select Input (S). That is:

1 Start bit
+ 2 Op-code bits
+ 9 Address bits
+ 8 Data bits

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 7. Absolute Maximum Ratings

Symbol	Parameter		Min.	Max.	Unit
T_{STG}	Storage Temperature		–65	150	°C
T_{LEAD}	Lead Temperature during Soldering	PDIP: 10 seconds SO: 20 seconds (max) [1] TSSOP: 20 seconds (max) [1]		260 235 235	°C
V_{OUT}	Output range (Q = V_{OH} or Hi-Z)		–0.3	V_{CC}+0.5	V
V_{IN}	Input range		–0.3	V_{CC}+1	V
V_{CC}	Supply Voltage		–0.3	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		–4000	4000	V

Note: 1. IPC/JEDEC J-STD-020A
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8. Operating Conditions (M93Cx6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
T_A	Ambient Operating Temperature (range 6)	–40	85	°C
	Ambient Operating Temperature (range 3)	–40	125	°C

Table 9. Operating Conditions (M93Cx6-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature (range 6)	–40	85	°C
	Ambient Operating Temperature (range 3)	–40	125	°C

Table 10. Operating Conditions (M93Cx6-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.8	5.5	V
T_A	Ambient Operating Temperature (range 6)	–40	85	°C

Table 11. AC Measurement Conditions (M93Cx6)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Pulse Voltages	0.4 V to 2.4 V		V
	Input Timing Reference Voltages	1.0 V and 2.0 V		V
	Output Timing Reference Voltages	0.8 V and 2.0 V		V

Note: 1. Output Hi-Z is defined as the point where data out is no longer driven.

Table 12. AC Measurement Conditions (M93Cx6-W and M93Cx6-R)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
	Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

Note: 1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 9. AC Testing Input Output Waveforms

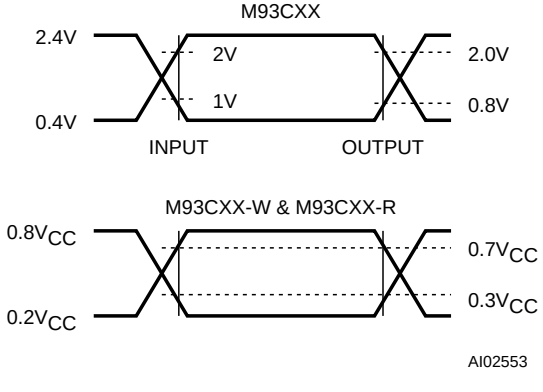


Table 13. Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF

Note: Sampled only, not 100% tested, at T_A=25°C and a frequency of 1 MHz.

Table 14. DC Characteristics (M93Cx6, temperature range 6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current	V_{CC} = 5V, S = V_{IH}, f = 1 MHz, Current Product [1]		1.5	mA
		V_{CC} = 5V, S = V_{IH}, f = 2 MHz, New Product [2]		2	mA
I_{CC1}	Supply Current (Stand-by)	V_{CC} = 5V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, Current Product [1]		50	µA
		V_{CC} = 5V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, New Product [2]		15	µA
V_{IL}	Input Low Voltage	V_{CC} = 5V ± 10%	–0.3	0.8	V
V_{IH}	Input High Voltage	V_{CC} = 5V ± 10%	2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	V_{CC} = 5V, I_{OH} = –400µA	2.4		V

Note: 1. Current product: identified by Process Identification letter F or M.
2. New product: identified by Process Identification letter W.

Table 15. DC Characteristics (M93Cx6, temperature range 3)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current	V_{CC} = 5V, S = V_{IH}, f = 1 MHz, Current Product [1]		1.5	mA
		V_{CC} = 5V, S = V_{IH}, f = 2 MHz, New Product [2]		2	mA
I_{CC1}	Supply Current (Stand-by)	V_{CC} = 5V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, Current Product [1]		50	µA
		V_{CC} = 5V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, New Product [2]		15	µA
V_{IL}	Input Low Voltage	V_{CC} = 5V ± 10%	–0.3	0.8	V
V_{IH}	Input High Voltage	V_{CC} = 5V ± 10%	2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	V_{CC} = 5V, I_{OH} = –400µA	2.4		V

Note: 1. Current product: identified by Process Identification letter F or M.
2. New product: identified by Process Identification letter W.

Table 16. DC Characteristics (M93Cx6-W, temperature range 6)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	V_{CC} = 5V, S = V_{IH}, f = 1 MHz, Current Product [1]		1.5	mA
		V_{CC} = 2.5V, S = V_{IH}, f = 1 MHz, Current Product [1]		1	mA
		V_{CC} = 5V, S = V_{IH}, f = 2 MHz, New Product [2]		2	mA
		V_{CC} = 2.5V, S = V_{IH}, f = 2 MHz, New Product [2]		1	mA
I_{CC1}	Supply Current (Stand-by)	V_{CC} = 2.5V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, Current Product [1]		10	µA
		V_{CC} = 2.5V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, New Product [2]		5	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.3	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
		V_{CC} = 2.5V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400µA	2.4		V
		V_{CC} = 2.5V, I_{OH} = –100µA	V_{CC}–0.2		V

Note: 1. Current product: identified by Process Identification letter F or M.
2. New product: identified by Process Identification letter W.

Table 17. DC Characteristics (M93Cx6-W, temperature range 3)

Symbol	Parameter	Test Condition	Min. [1]	Max. [1]	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	V_{CC} = 5V, S = V_{IH}, f = 2 MHz		2	mA
		V_{CC} = 2.5V, S = V_{IH}, f = 2 MHz		1	mA
I_{CC1}	Supply Current (Stand-by)	V_{CC} = 2.5V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		5	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.3	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
		V_{CC} = 2.5V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400µA	2.4		V
		V_{CC} = 2.5V, I_{OH} = –100µA	V_{CC}–0.2		V

Note: 1. New product: identified by Process Identification letter W.

Table 18. DC Characteristics (M93Cx6-R)

Symbol	Parameter	Test Condition	Min. [1]	Max. [1]	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	V_{CC} = 5V, S = V_{IH}, f = 2 MHz		2	mA
		V_{CC} = 1.8V, S = V_{IH}, f = 1 MHz		1	mA
I_{CC1}	Supply Current (Stand-by)	V_{CC} = 1.8V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		2	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.3	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)		0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 1.8V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 1.8V, I_{OH} = –100µA	V_{CC}–0.2		V

Note: 1. This product is under development. For more infomation, please contact your nearest ST sales office.

Table 19. AC Characteristics (M93Cx6, temperature range 6 or 3)

Test conditions specified in Table 11 and Table 8							
Symbol	**Alt.**	**Parameter**	**Min.[3]**	**Max.[3]**	**Min.[4]**	**Max.[4]**	**Unit**
f_C	f_{SK}	Clock Frequency	D.C.	1	D.C.	2	MHz
t_{SLCH}		Chip Select Low to Clock High	250		50		ns
t_{SHCH}	t_{CSS}	Chip Select Set-up Time M93C46, M93C56, M93C66	50		50		ns
		Chip Select Set-up time M93C76, M93C86	100		50		ns
t_{SLSH}[2]	t_{CS}	Chip Select Low to Chip Select High	250		200		ns
t_{CHCL}[1]	t_{SKH}	Clock High Time	250		200		ns
t_{CLCH}[1]	t_{SKL}	Clock Low Time	250		200		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	100		50		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	100		50		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	100		50		ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		0		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		400		200	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		200		100	ns
t_{CHQL}	t_{PD0}	Delay to Output Low		400		200	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		400		200	ns
t_W	t_{WP}	Erase/Write Cycle time		10		5	ms

Note: 1. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.
2. Chip Select Input (S) must be brought Low for a minimum of tSLSH between consecutive instruction cycles.
3. Current product: identified by Process Identification letter F or M.
4. New product: identified by Process Identification letter W.

Table 20. AC Characteristics (M93Cx6-W, temperature range 6)

Test conditions specified in Table 12 and Table 9							
Symbol	**Alt.**	**Parameter**	**Min.[3]**	**Max.[3]**	**Min.[4]**	**Max.[4]**	**Unit**
f_C	f_{SK}	Clock Frequency	D.C.	1	D.C.	2	MHz
t_{SLCH}		Chip Select Low to Clock High	250		50		ns
t_{SHCH}	t_{CSS}	Chip Select Set-up Time	100		50		ns
t_{SLSH}[2]	t_{CS}	Chip Select Low to Chip Select High	1000		200		ns
t_{CHCL}[1]	t_{SKH}	Clock High Time	350		200		ns
t_{CLCH}[1]	t_{SKL}	Clock Low Time	250		200		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	100		50		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	100		50		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	100		50		ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		0		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		400		200	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		200		100	ns
t_{CHQL}	t_{PD0}	Delay to Output Low		400		200	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		400		200	ns
t_W	t_{WP}	Erase/Write Cycle time		10		5	ms

Note: 1. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.
2. Chip Select Input (S) must be brought Low for a minimum of tSLSH between consecutive instruction cycles.
3. Current product: identified by Process Identification letter F or M.
4. New product: identified by Process Identification letter W.

Table 21. AC Characteristics (M93Cx6-W, temperature range 3)

Test conditions specified in Table 12 and Table 9					
Symbol	**Alt.**	**Parameter**	**Min.[3]**	**Max.[3]**	**Unit**
f_C	f_{SK}	Clock Frequency	D.C.	2	MHz
t_{SLCH}		Chip Select Low to Clock High	50		ns
t_{SHCH}	t_{CSS}	Chip Select Set-up Time	50		ns
t_{SLSH}[2]	t_{CS}	Chip Select Low to Chip Select High	200		ns
t_{CHCL}[1]	t_{SKH}	Clock High Time	200		ns
t_{CLCH}[1]	t_{SKL}	Clock Low Time	200		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	50		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	50		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	50		ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		200	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		100	ns
t_{CHQL}	t_{PD0}	Delay to Output Low		200	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		200	ns
t_W	t_{WP}	Erase/Write Cycle time		5	ms

Note: 1. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.
2. Chip Select Input (S) must be brought Low for a minimum of tSLSH between consecutive instruction cycles.
3. New product: identified by Process Identification letter W.

Table 22. AC Characteristics (M93Cx6-R)

Test conditions specified in Table 12 and Table 10					
Symbol	**Alt.**	**Parameter**	**Min.[3]**	**Max.[3]**	**Unit**
f_C	f_{SK}	Clock Frequency	D.C.	1	MHz
t_{SLCH}		Chip Select Low to Clock High	250		ns
t_{SHCH}	t_{CSS}	Chip Select Set-up Time	50		ns
t_{SLSH}[2]	t_{CS}	Chip Select Low to Chip Select High	250		ns
t_{CHCL}[1]	t_{SKH}	Clock High Time	250		ns
t_{CLCH}[1]	t_{SKL}	Clock Low Time	250		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	100		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	100		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	100		ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		400	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		200	ns
t_{CHQL}	t_{PD0}	Delay to Output Low		400	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		400	ns
t_W	t_{WP}	Erase/Write Cycle time		10	ms

Note: 1. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.
2. Chip Select Input (S) must be brought Low for a minimum of tSLSH between consecutive instruction cycles.
3. This product is under development. For more infomation, please contact your nearest ST sales office.

Figure 10. Synchronous Timing (Start and Op-Code Input)

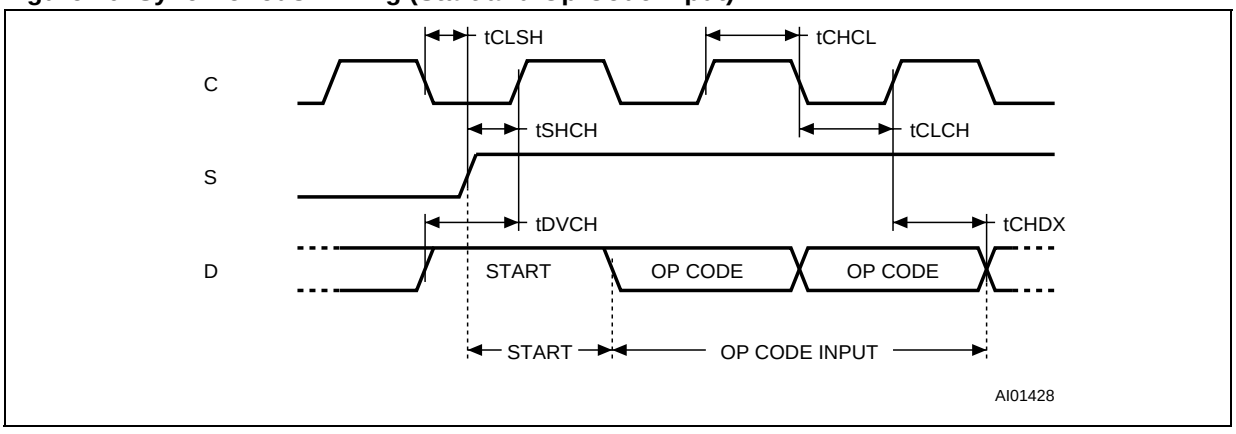


Figure 11. Synchronous Timing (Read or Write)

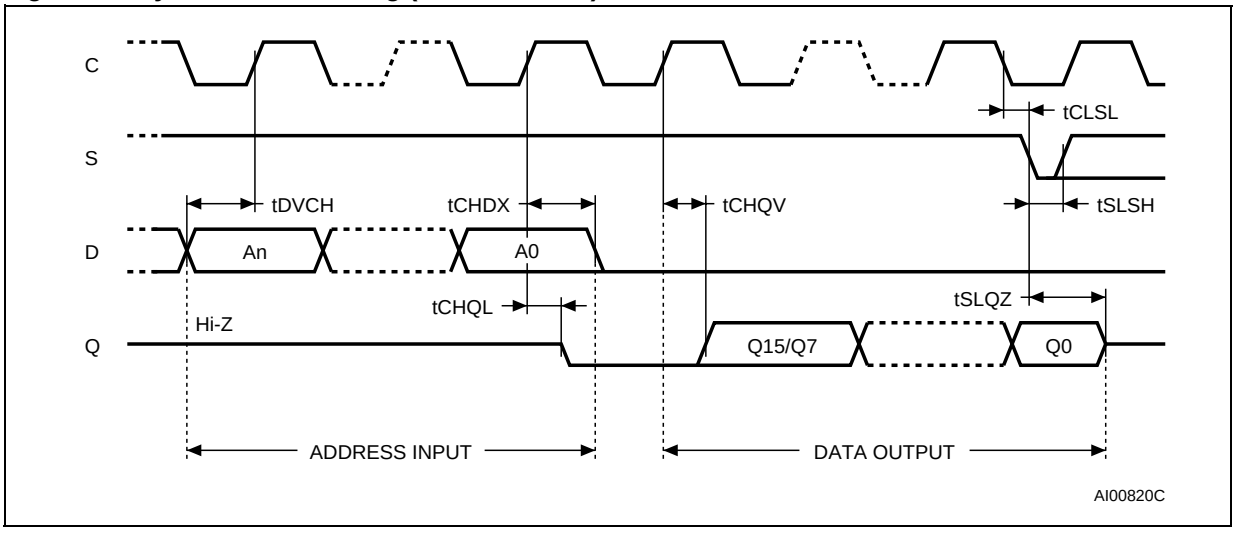
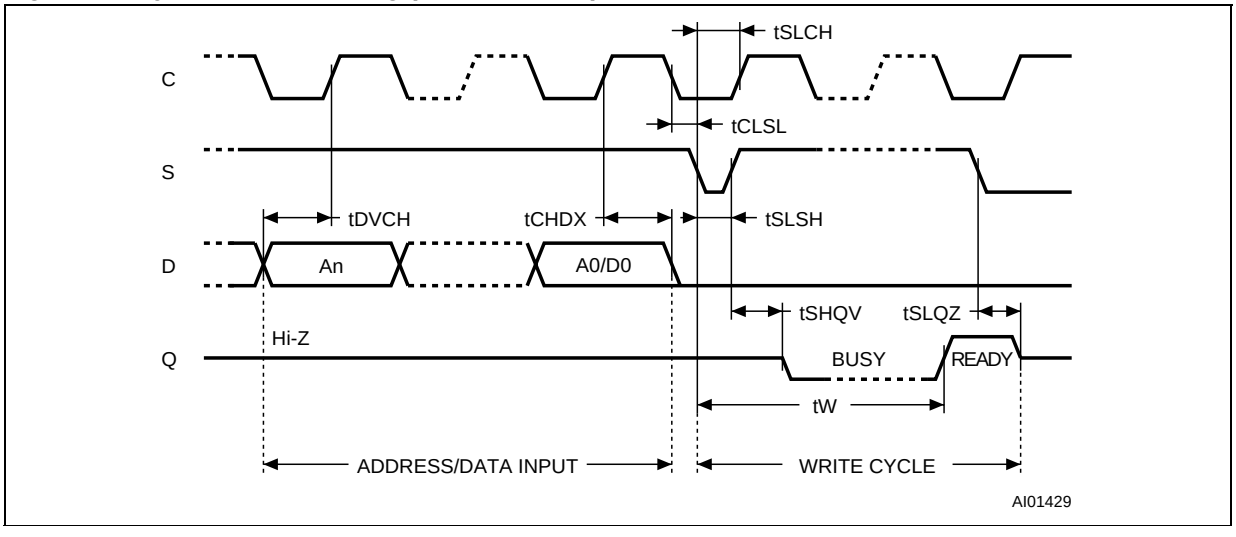
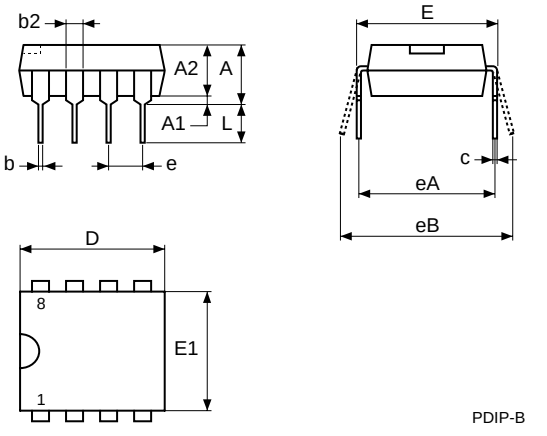


Figure 12. Synchronous Timing (Read or Write)



PACKAGE MECHANICAL

PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, Package Outline

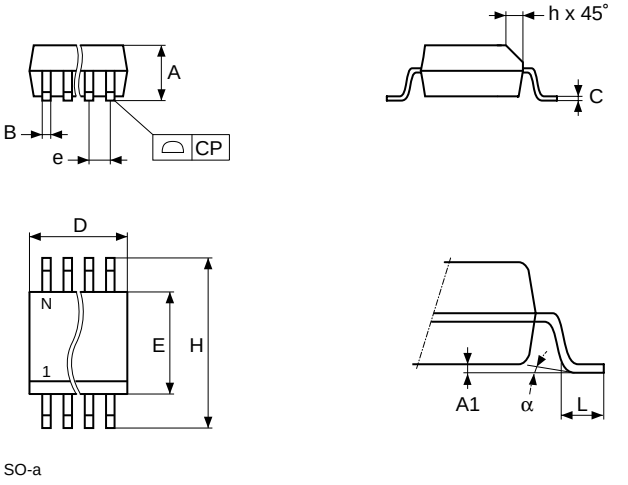


Notes: 1. Drawing is not to scale.

PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, Package Mechanical Data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.210
A1		0.38			0.015	
A2	3.30	2.92	4.95	0.130	0.115	0.195
b	0.46	0.36	0.56	0.018	0.014	0.022
b2	1.52	1.14	1.78	0.060	0.045	0.070
c	0.25	0.20	0.36	0.010	0.008	0.014
D	9.27	9.02	10.16	0.365	0.355	0.400
E	7.87	7.62	8.26	0.310	0.300	0.325
E1	6.35	6.10	7.11	0.250	0.240	0.280
e	2.54	–	–	0.100	–	–
eA	7.62	–	–	0.300	–	–
eB			10.92			0.430
L	3.30	2.92	3.81	0.130	0.115	0.150

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Outline



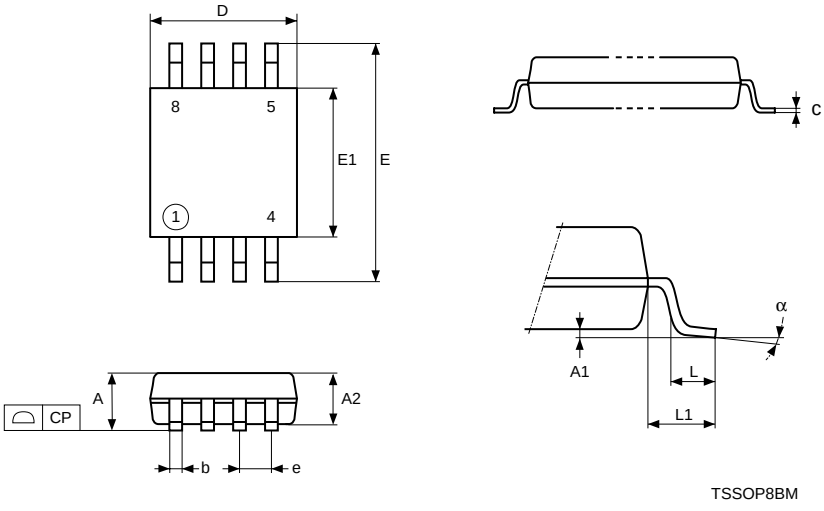
SO-a

Note: Drawing is not to scale.

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Mechanical Data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

TSSOP8 3x3mm² – 8 lead Thin Shrink Small Outline, 3x3mm² body size, Package Outline

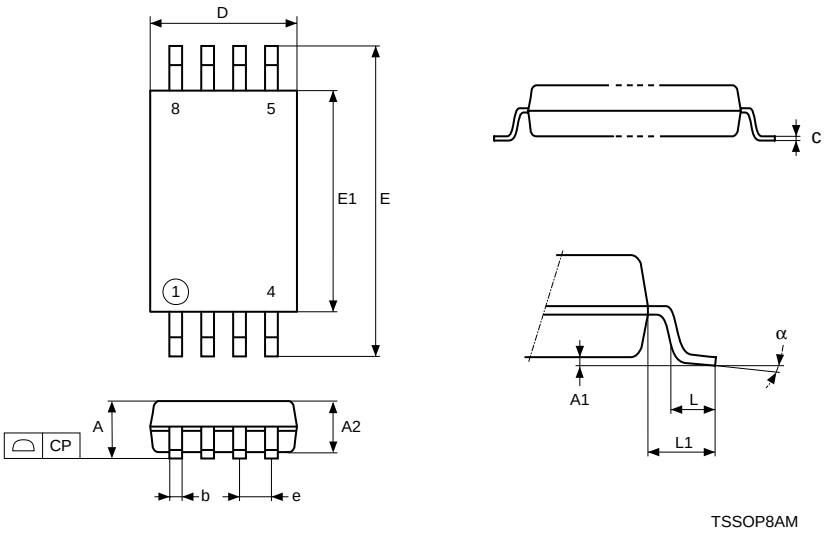


Notes: 1. Drawing is not to scale.

TSSOP8 3x3mm² – 8 lead Thin Shrink Small Outline, 3x3mm² body size, Package Mechanical Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.100			0.0433
A1		0.050	0.150		0.0020	0.0059
A2	0.850	0.750	0.950	0.0335	0.0295	0.0374
b		0.250	0.400		0.0098	0.0157
c		0.130	0.230		0.0051	0.0091
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
E	4.900	4.650	5.150	0.1929	0.1831	0.2028
E1	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
CP			0.100			0.0039
L	0.550	0.400	0.700	0.0217	0.0157	0.0276
L1	0.950			0.0374		
α		0°	6°		0°	6°

TSSOP8 – 8 lead Thin Shrink Small Outline, Package Outline



Notes: 1. Drawing is not to scale.

TSSOP8 – 8 lead Thin Shrink Small Outline, Package Mechanical Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

PART NUMBERING

Table 23. Ordering Information Scheme

Example: M93C86 – T W MN 6 T

Device Type

M93 = MICROWIRE serial access EEPROM

Device Function

86 = 16 Kbit (2048 x 8)

76 = 8 Kbit (1024 x 8)

66 = 4 Kbit (512 x 8)

56 = 2 Kbit (256 x 8)

46 = 1 Kbit (128 x 8)

06[2] = 256 bit (32 x 8)

Turned Die

blank = Normal (unturned) Die

T[4] = 90° Turned Die

Operating Voltage

blank = V_{CC} = 4.5 to 5.5V

W = V_{CC} = 2.5 to 5.5V

R = V_{CC} = 1.8 to 5.5V

Package

BN = PDIP8

MN = SO8 (150 mil width)

DW = TSSOP8 (169 mil width)

DS[3] = TSSOP8 (3x3mm body size)

Temperature Range

6 = –40 to 85 °C

3[1] = –40 to 125 °C

Option

T = Tape & Reel Packing

Note: 1. Produced with High Reliability Certified Flow (HRCF).
2. M93C06 is "Not for New Design".
3. Available only on new products: identified by the Process Identification letter W.
4. Turned die option is not available for all devices. Please contact your nearest STMicroelectronics Sales Office.

Devices are shipped from the factory with the memory content set at all 1s (FFFFh for x16, FFh for x8).

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

Table 24. How to Identify Current and New Products by the Process Identification Letter

Markings on Current Products[1]	Markings on New Products[1]
M93C46W6 AYWW**F** (or AYWW**M**)	M93C46W6 AYWW**W**

Note: 1. This example comes from the S08 package. Other packages have similar information. For further information, please ask your ST Sales Office for Process Change Notice PCN MPG/EE/0059 (PCEE0059).

REVISION HISTORY

Table 25. Document Revision History

Date	Rev.	Description of Revision
04-Feb-2003	2.0	Document reformatted, and reworded, using the new template. Temperature range 1 removed. TSSOP8 (3x3mm) package added. New products, identified by the process letter W, added, with fc(max) increased to 1MHz for -R voltage range, and to 2MHz for all other ranges (and corresponding parameters adjusted)
26-Mar-2003	2.1	Value of standby current (max) corrected in DC characteristics tables for -W and -R ranges V_{OUT} and V_{IN} separated from V_{IO} in the Absolute Maximum Ratings table
04-Apr-2003	2.2	Values corrected in AC characteristics tables for -W range (tSLSH, tDVCH, tCLSL) for devices with Process Identification Letter W
23-May-2003	2.3	Standby current corrected for -R range
27-May-2003	2.4	Turned die option re-instated in Ordering Information Scheme