SYC SEMICONDUCTORES Y COMPONENTES

# Quad EIA-485 Line Drivers with Three-State Outputs

The ON Semiconductor MC75172B/174B Quad Line drivers are differential high speed drivers designed to comply with the EIA−485 Standard. Features include three−state outputs, thermal shutdown, and output current limiting in both directions. These devices also comply with EIA−422−A, and CCITT Recommendations V.11 and X.27.

The MC75172B/174B are optimized for balanced multipoint bus transmission at rates in excess of 10 MBPS. The outputs feature wide common mode voltage range, making them suitable for party line applications in noisy environments. The current limit and thermal shutdown features protect the devices from line fault conditions. These devices offer optimum performance when used with the MC75173 and MC75175 line receivers.

Both devices are available in 16−pin plastic PDIP and 20−pin wide body surface mount packages.

### Features

- Meets EIA−485 Standard for Party Line Operation
- Meets EIA−422−A and CCITT Recommendations V.11 and X.27
- Operating Ambient Temperature: −40°C to +85°C
- High Impedance Outputs
- Common Mode Output Voltage Range: −7.0 to 12 V
- Positive and Negative Current Limiting
- Transmission Rates in Excess of 10 MBPS
- Thermal Shutdown at 150°C Junction Temperature, (±20°C)
- Single 5.0 V Supply
- Pin Compatible with TI SN75172/4 and NS μA96172/4
- Interchangeable with MC3487 and AM26LS31 for EIA−422−A Applications
- Pb−Free Packages are Available*

### MAXIMUM RATING

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | −0.5, +7.0 | Vdc |
| Input Voltage (Data, Enable) | $V_{in}$ | +7.0 | Vdc |
| Input Current (Data, Enable) | $I_{in}$ | −24 | mA |
| Applied Output Voltage, when in 3−State Condition ($V_{CC}$ = 5.0 V) | $V_{za}$ | −10, +14 | Vdc |
| Applied Output Voltage, when $V_{CC}$ = 0 V | $V_{zb}$ | ±14 | Vdc |
| Output Current | $I_O$ | Self−Limiting | − |
| Storage Temperature | $T_{stg}$ | −65, +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

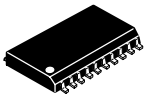
1. Devices should not be operated at these limits. The “Recommended Operating Conditions” table provides for actual device operation.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

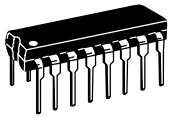
75174

## QUAD EIA−485 LINE DRIVERS

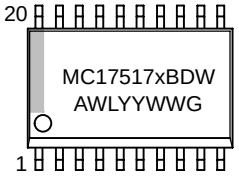
**SOIC−20 WB**
**DW SUFFIX**
**CASE 751D**




**PDIP−16**
**P SUFFIX**
**CASE 648**




### MARKING DIAGRAMS







x = 2 or 4
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

**RECOMMENDED OPERATING CONDITIONS**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | +4.75 | +5.0 | +5.25 | Vdc |
| Input Voltage (All Inputs) | $V_{in}$ | 0 | − | $V_{CC}$ | Vdc |
| Output Voltage in 3−State Condition, or when $V_{CC}$ = 0 V | $V_{cm}$ | −7.0 | − | +12 | Vdc |
| Output Current (Normal data transmission) | $I_O$ | −65 | − | +65 | mA |
| Operating Ambient Temperature (see text)<br>EIA−485<br>EIA−422 | $T_A$ | <br>−40<br>0 | − | +85 | °C |

2. All limits are not necessarily functional concurrently.

**ELECTRICAL CHARACTERISTICS** (−40°C ≤ $T_A$ ≤ 85°C, 4.75 V ≤ $V_{CC}$ ≤ 5.25 V, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage<br>Single−Ended Voltage | | | | | Vdc |
| $I_O$ = 0 | $V_O$ | 0 | − | 6.0 | |
| High @ $I_O$ = −33 mA | $V_{OH}$ | − | 4.0 | − | |
| Low @ $I_O$ = +33 mA | $V_{OL}$ | − | 1.6 | − | |
| Differential Voltage | | | | | |
| Open Circuit ($I_O$ = 0) | $\|V_{OD1}\|$ | 1.5 | 3.4 | 6.0 | |
| $R_L$ = 54 Ω (Figure 1) | $\|V_{OD2}\|$ | 1.5 | 2.3 | 5.0 | |
| Change in Differential*, $R_L$ = 54 Ω (Figure 1) | $\|\Delta V_{OD2}\|$ | − | 5.0 | 200 | mVdc |
| Differential Voltage, $R_L$ = 100 Ω (Figure 1) | $\|V_{OD2A}\|$ | − | 2.2 | − | Vdc |
| Change in Differential*, $R_L$ = 100 Ω (Figure 1) | $\|\Delta V_{OD2A}\|$ | − | 5.0 | 200 | mVdc |
| Differential Voltage, −7.0 V ≤ $V_{cm}$ ≤ 12 V (Figure 2) | $\|V_{OD3}\|$ | 1.5 | − | 5.0 | Vdc |
| Change in Differential*, −7.0 V ≤ $V_{cm}$ ≤ 12 V (Figure 2) | $\|\Delta V_{OD3}\|$ | − | 5.0 | 200 | mVdc |
| Offset Voltage, $R_L$ = 54 Ω (Figure 1) | $V_{OS}$ | − | 2.9 | − | Vdc |
| Change in Offset*, $R_L$ = 54 Ω (Figure 1) | $\|\Delta V_{OS}\|$ | − | 5.0 | 200 | mVdc |
| Output Current (Each Output)<br>Power Off Leakage, $V_{CC}$ = 0, −7.0 V ≤ $V_O$ ≤ 12 V | $I_{O(off)}$ | −50 | 0 | +50 | μA |
| Leakage in 3−State Mode, −7.0 V ≤ $V_O$ ≤ 12 V | $I_{OZ}$ | −50 | 0 | +50 | |
| Short Circuit Current to Ground | $I_{OSR}$ | −150 | − | +150 | mA |
| Short Circuit Current, −7.0 V ≤ $V_O$ ≤ 12 V | $I_{OS}$ | −250 | − | +250 | |
| Inputs<br>Low Level Voltage (Pins 4 & 12, MC75174B only) | $V_{IL(A)}$ | 0 | − | 0.7 | Vdc |
| Low Level Voltage (All Other Pins) | $V_{IL(B)}$ | 0 | − | 0.8 | |
| High Level Voltage (All Inputs) | $V_{IH}$ | 2.0 | − | $V_{CC}$ | |
| Current @ $V_{in}$ = 2.7 V (All Inputs) | $I_{IH}$ | − | 0.2 | 20 | μA |
| Current @ $V_{in}$ = 0.5 V (All Inputs) | $I_{IL}$ | −100 | −15 | − | |
| Clamp Voltage (All Inputs, $I_{in}$ = −18 mA) | $V_{IK}$ | −1.5 | − | − | Vdc |
| Thermal Shutdown Junction Temperature | $T_{jts}$ | − | +150 | − | °C |
| Power Supply Current (Outputs Open, $V_{CC}$ = 5.25 V)<br>Outputs Enable | $I_{CC}$ | − | 60 | 70 | mA |
| Outputs Disabled | | − | 30 | 40 | |

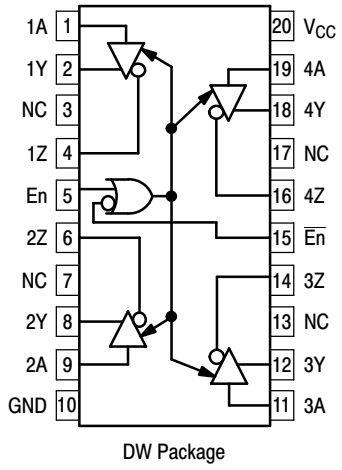
3. *$V_{in}$ switched from 0.8 to 2.0 V. Typical values determined at 25°C ambient and 5.0 V supply.

**TIMING CHARACTERISTICS** ($T_A$ = 25°C, $V_{CC}$ = 5.0 V)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay − Input to Single−ended Output (Figure 3) | | | | | ns |
| Output Low−to−High | $t_{PLH}$ | − | 23 | 30 | |
| Output High−to−Low | $t_{PHL}$ | − | 18 | 30 | |
| Propagation Delay − Input to Differential Output (Figure 4) | | | | | ns |
| Input Low−to−High | $t_{PLH(D)}$ | − | 15 | 25 | |
| Input High−to−Low | $t_{PHL(D)}$ | − | 17 | 25 | |
| Differential Output Transition Time (Figure 4) | $t_{dr}$, $t_{df}$ | − | 19 | 25 | ns |
| Skew Timing | | | | | ns |
| $\lvert t_{PLHD} - t_{PHLD} \rvert$ for Each Driver | $t_{SK1}$ | − | 0.2 | − | |
| Max − Min $t_{PLHD}$ Within a Package | $t_{SK2}$ | − | 1.5 | − | |
| Max − Min $t_{PHLD}$ Within a Package | $t_{SK3}$ | − | 1.5 | − | |
| Enable Timing | | | | | ns |
| Single−ended Outputs (Figure 5) | | | | | |
| Enable to Active High Output | $t_{PZH(E)}$ | − | 48 | 60 | |
| Enable to Active Low Output | $t_{PZL(E)}$ | − | 20 | 30 | |
| Active High to Disable (using Enable) | $t_{PHZ(E)}$ | − | 35 | 45 | |
| Active Low to Disable (using Enable) | $t_{PLZ(E)}$ | − | 30 | 50 | |
| $\overline{\text{Enable}}$ to Active High Output (MC75172B only) | $t_{PZH(E)}$ | − | 58 | 70 | |
| $\overline{\text{Enable}}$ to Active Low Output (MC75172B only) | $t_{PZL(E)}$ | − | 28 | 35 | |
| Active High to Disable (using $\overline{\text{Enable}}$, MC75172B only) | $t_{PHZ(E)}$ | − | 38 | 50 | |
| Active Low to Disable (using $\overline{\text{Enable}}$, MC75172B only) | $t_{PLZ(E)}$ | − | 36 | 50 | |
| Differential Outputs (Figure 6) | | | | | ns |
| Enable to Active Output | $t_{PZD(E)}$ | − | 47 | − | |
| $\overline{\text{Enable}}$ to Active Output (MC75172B only) | $t_{PZD(E)}$ | − | 56 | − | |
| Enable to 3−State Output | $t_{PDZ(E)}$ | − | 32 | − | |
| $\overline{\text{Enable}}$ to 3−State Output (MC75172B only) | $t_{PDZ(E)}$ | − | 40 | − | |

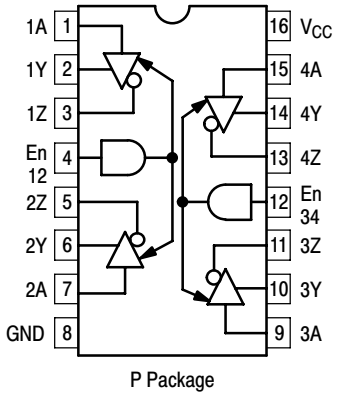
**PIN CONNECTIONS**

**MC75172B**

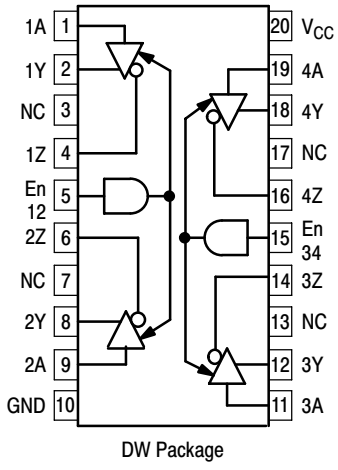



DW Package

**MC75174B**




P Package




DW Package

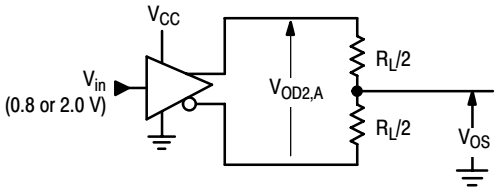



**Figure 1. $V_{DD}$ Measurement**

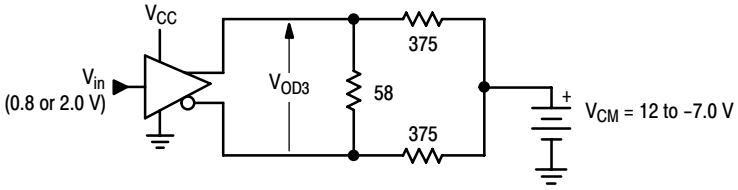



**Figure 2. Common Mode Test**

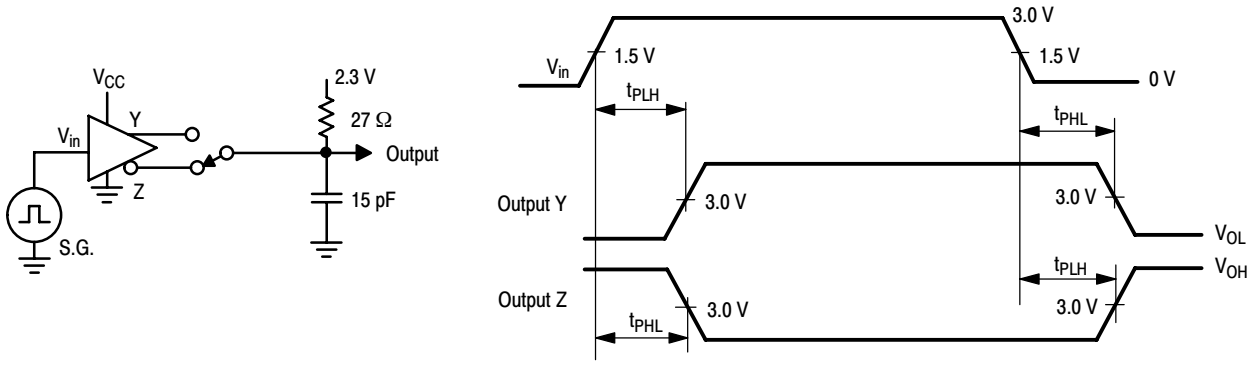
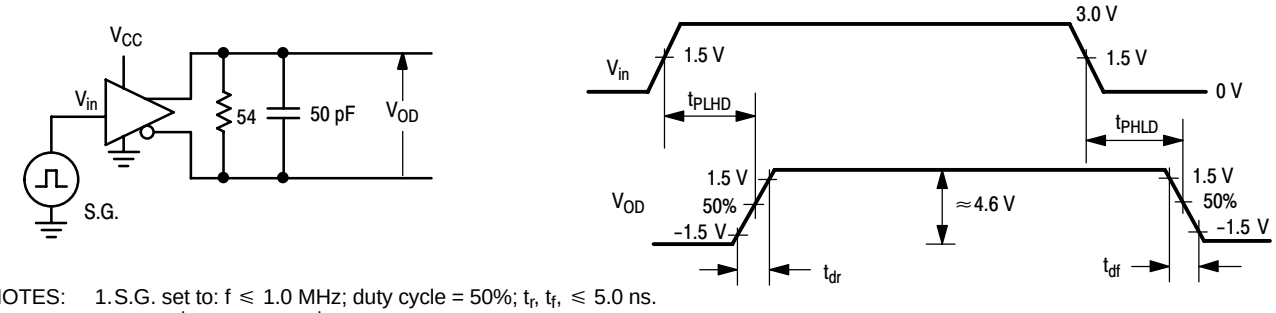



**Figure 3. Propagation Delay, Single−Ended Outputs**




NOTES: 1. S.G. set to: f ⩽ 1.0 MHz; duty cycle = 50%; $t_r$, $t_f$, ⩽ 5.0 ns.
2. $t_{SK1} = |t_{PLHD} - t_{PHLD}|$ for each driver.
3. $t_{SK2}$ computed by subtracting the shortest $t_{PLHD}$ from the longest $t_{PLHD}$ of the 4 drivers within a package.
4. $t_{SK3}$ computed by subtracting the shortest $t_{PHLD}$ from the longest $t_{PHLD}$ of the 4 drivers within a package.

**Figure 4. Propagation Delay, Differential Outputs**

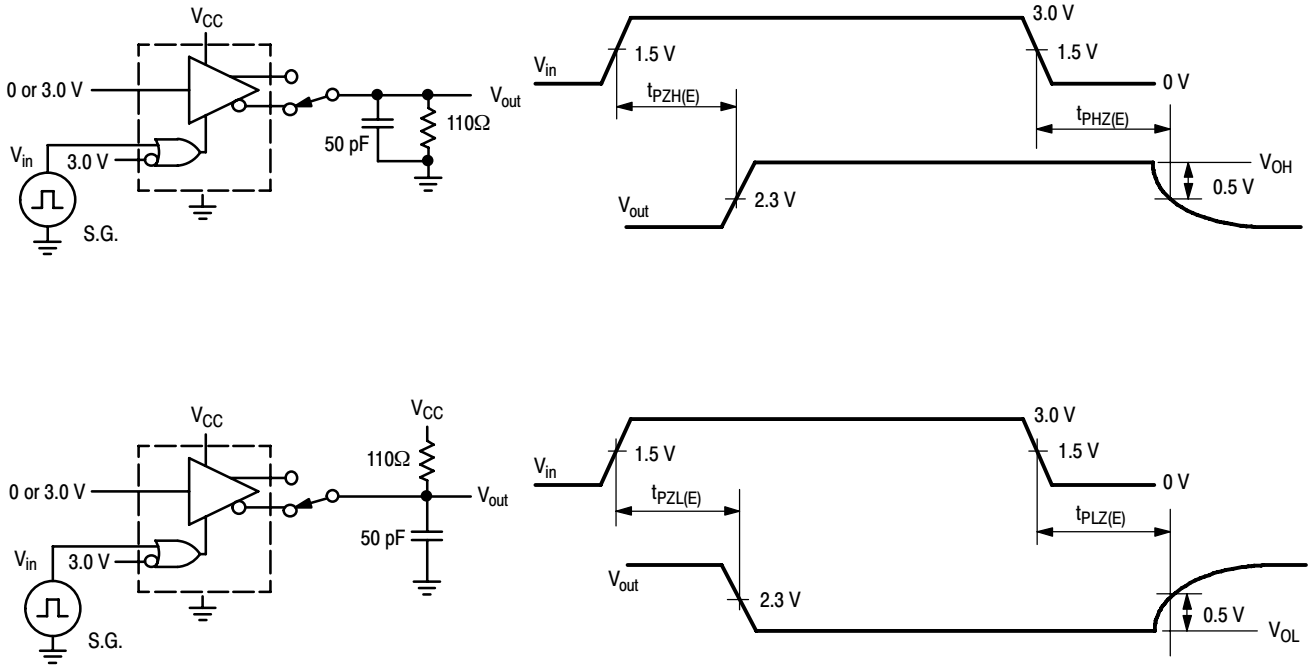
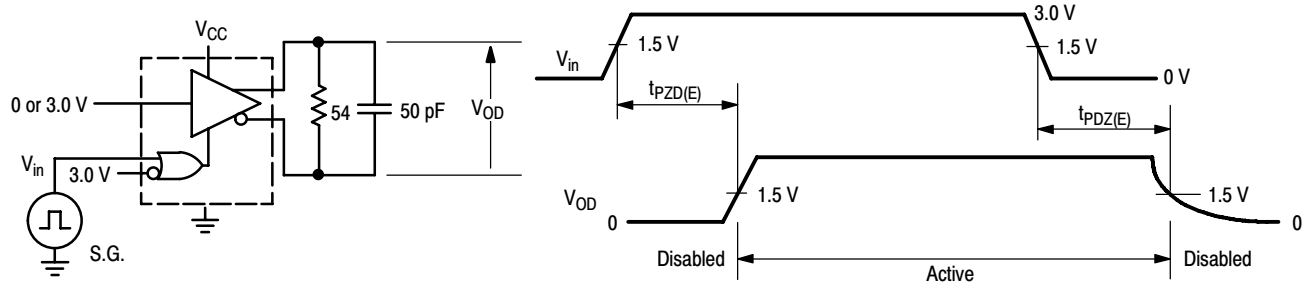



**Figure 5. Enable Timing, Single−Ended Outputs**




NOTES: 1. S.G. set to: f ⩽ 1.0 MHz; duty cycle = 50%; $t_f$, $t_f$, ⩽ 5.0 ns.
2. $V_{in}$ is inverted for $\overline{\text{Enable}}$ measurements.

**Figure 6. Enable Timing, Differential Outputs**

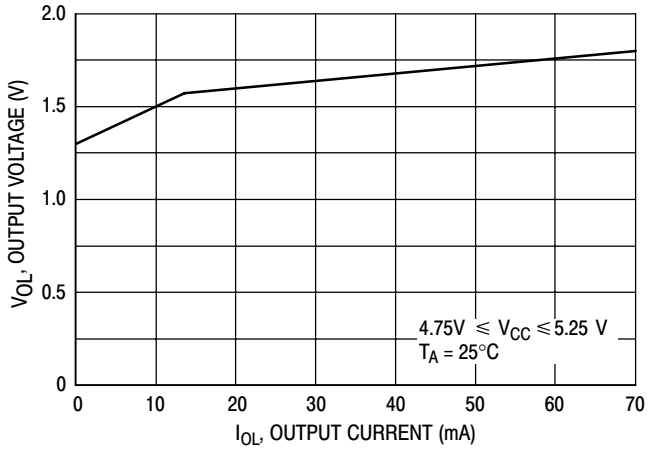



**Figure 7. Single−Ended Output Voltage versus Output Sink Current**

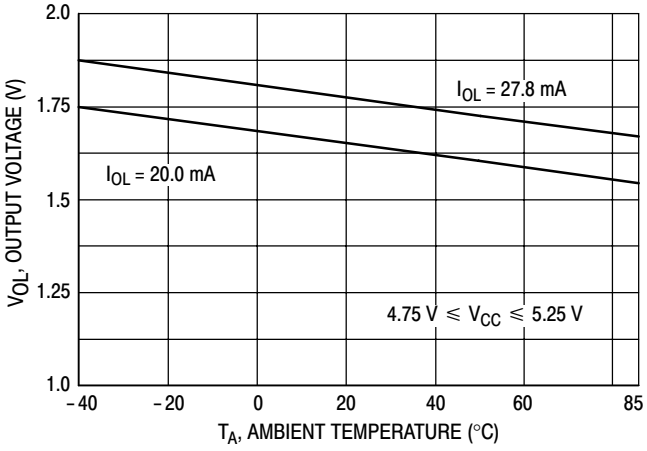



**Figure 8. Single−Ended Output Voltage versus Temperature**

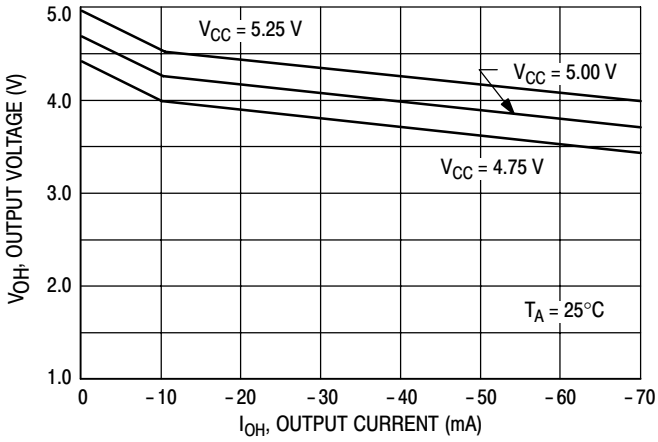



**Figure 9. Single−Ended Output Voltage versus Output Source Current**

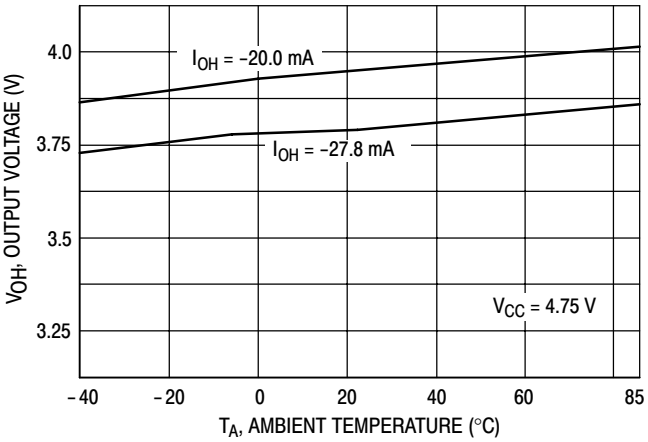



**Figure 10. Single−Ended Output Voltage versus Temperature**

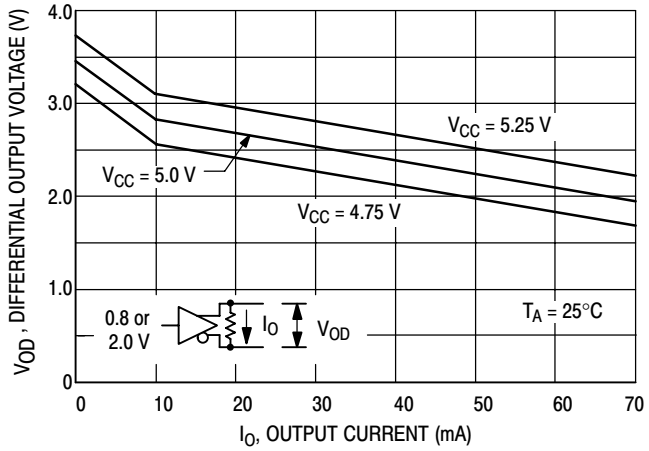



**Figure 11. Output Differential Voltage versus Load Current**

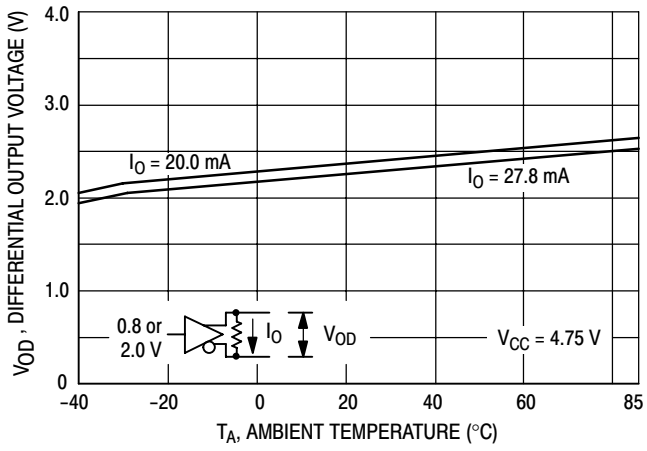



**Figure 12. Output Differential Voltage versus Temperature**

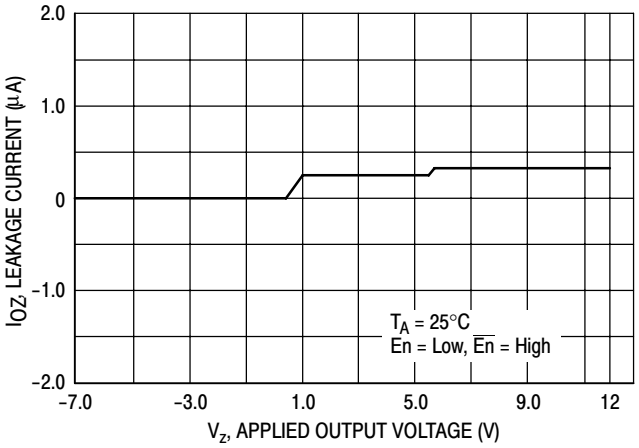



**Figure 13. Output Leakage Current versus Output Voltage**

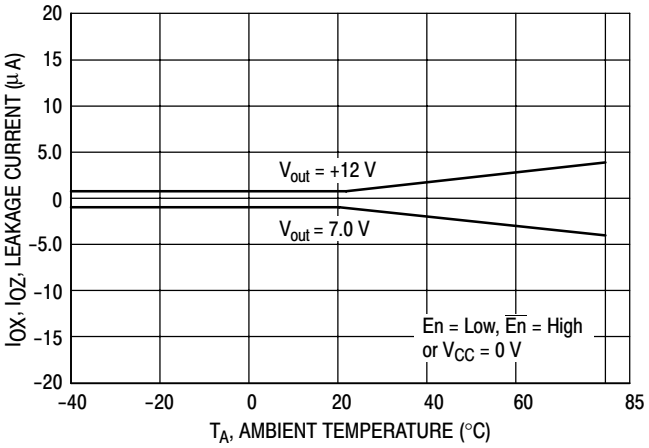



**Figure 14. Output Leakage Current versus Temperature**

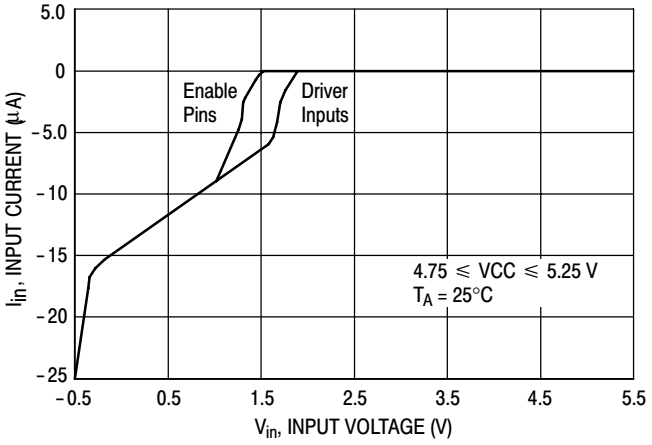



**Figure 15. Input Current versus Input Voltage**

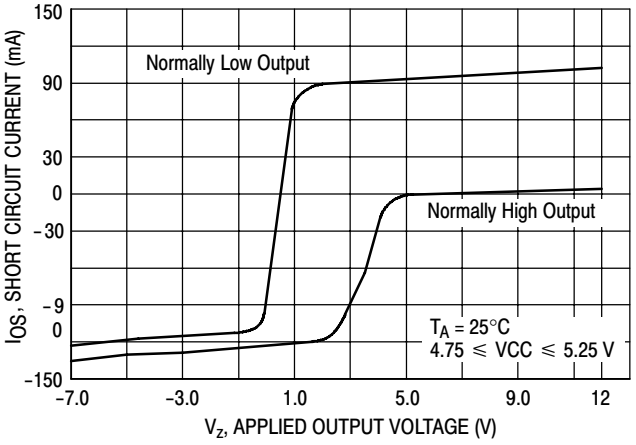



**Figure 16. Short Circuit Current versus Common Mode Voltage**

## APPLICATIONS INFORMATION

### Description

The MC75172B and MC75174B are differential line drivers designed to comply with EIA−485 Standard (April 1983) for use in balanced digital multipoint systems containing multiple drivers. The drivers also comply with EIA−422−A and CCITT Recommendations V.11 and X.27. The drivers meet the EIA−485 requirement for protection from damage in the event that two or more drivers attempt to transmit data simultaneously on the same cable. Data rates in excess of 10 MBPS are possible, depending on the cable length and cable characteristics. A single power supply, 5.0 V, ±5%, is required at a nominal current of 60 mA, plus load currents.

### Outputs

Each output (when active) will be a low or a high voltage, which depends on the input state and the load current (see Table 1, 2 and Figures 7 to 10). The graphs apply to each driver, regardless of how many other drivers within the package are supplying load current.

**Table 1. MC75172B Truth Table**

| | Enables | | Outputs | |
|---|---|---|---|---|
| Data Input | EN | $\overline{EN}$ | Y | Z |
| H | H | X | H | L |
| L | H | X | L | H |
| H | X | L | H | L |
| L | X | L | L | H |
| X | L | H | Z | Z |

**Table 2. MC75174B Truth Table**

| | | Outputs | |
|---|---|---|---|
| Data Input | Enable | Y | Z |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |

H = Logic high, L = Logic low, X = Irrelevant, Z = High impedance

The two outputs of a driver are always complementary. A “high” output can only source current out, while a “low” output can only sink current (except for short circuit current − see Figure 16).

The outputs will be in the high impedance mode when:

a) the Enable inputs are set according to Table 1 or 2;

b) $V_{CC}$ is less than 1.5 V;

c) the junction temperature exceeds the trip point of the thermal shutdown circuit (see below). When in this condition, the output’s source and sink capability are shut off, and only leakage currents will flow (see Figures 13, 14). Disabled outputs may be taken to any voltage between −7.0 V and 12 V without damage.

The drivers are protected from short circuits by two methods:

a) Current limiting is provided at each output, in both the source and sink direction, for shorts to any voltage within the range of 12 V to −7.0 V, with respect to circuit ground (see Figure 16). The short circuit current will flow until the fault is removed, or until the thermal shutdown circuit activates (see below). The current limiting circuit has a negative temperature coefficient and requires no resetting upon removal of the fault condition.

b) A thermal shutdown circuit disables the outputs when the junction temperature reaches 150°C, ±20°C. The thermal shutdown circuit has a hysteresis of ≈ 12°C to prevent oscillations. When this circuit activates, the output stage of each driver is put into the high impedance mode, thereby shutting off the output currents. The remainder of the internal circuitry remains biased. The outputs will become active once again as the IC cools down.

### Driver Inputs

The driver inputs determine the state of the outputs in accordance with Tables 1 and 2. The driver inputs have a nominal threshold of 1.2 V, and their voltage must be kept within the range of 0 V to $V_{CC}$ for proper operation. If the voltage is taken more than 0.5 V below ground, excessive currents will flow, and proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The characteristics of the driver inputs are shown in Figure 15. This graph is not affected by the state of the Enable pins.

### Enable Logic

Each driver’s outputs are active when the Enable inputs (Pins 4 and 12) are true according to Tables 1 and 2.

The Enable inputs have a nominal threshold of 1.2 V and their voltage must be kept within the range of 0 V to $V_{CC}$ for proper operation. If the voltage is taken more than 0.5 V below ground, excessive currents will flow, and proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The Enable input characteristics are shown in Figure 15.

### Operating Temperature Range

The minimum ambient operating temperature is listed as −40°C to meet EIA−485 specifications, and 0°C to meet EIA−422−A specifications. The higher $V_{OD}$ required by EIA−422−A is the reason for the narrower temperature range.

The maximum ambient operating temperature (applicable to both EIA−485 and EIA−422−A) is listed as 85°C. However, a lower ambient may be required depending on system use (i.e. specifically how many drivers within a package are used) and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$PD_{max} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

where: $R_{\theta JA}$ = package thermal resistance (typical 70°C/W for the DIP package, 85°C/W for SOIC package);
$T_{Jmax}$ = max. operating junction temperature, and
$T_A$ = ambient temperature.

Since the thermal shutdown feature has a trip point of 150°C, ±20°C, $T_{Jmax}$ is selected to be 130°C. The power dissipated within the package is calculated from:

PD = {[($V_{CC}$ − $V_{OH}$) • $I_{OH}$] + $V_{OL}$ • $I_{OL}$)} each driver + ($V_{CC}$ • $I_{CC}$)

where: $V_{CC}$ = the supply voltage;
$V_{OH}$, $V_{OL}$ are measured or estimated from Figures 7 to 10;
$I_{CC}$ = the quiescent power supply current (typical 60 mA).

As indicated in the equation, the first term (in brackets) must be calculated and summed for each of the four drivers, while the last term is common to the entire package.

*Example 1:* $T_A$ = 25°C, $I_{OL}$ = $I_{OH}$ = 55 mA for each driver, $V_{CC}$ = 5.0 V, DIP package. How many drivers per package can be used?

Maximum allowable power dissipation is:

$$PD_{max} = \frac{130°C - 25°C}{70°C/W} = 1.5\ W$$

Since the power supply current of 60 mA dissipates 300 mW, that leaves 1.2 W (1.5 W − 0.3 W) for the drivers. From Figures 7 and 9, $V_{OL}$ ≈1.75 V, and $V_{OH}$ ≈3.85 V. The power dissipated in each driver is:

{(5.0 − 3.85) • 0.055} + (1.75 • 0.055) = 160 mW.

Since each driver dissipates 160 mW, the four drivers per package could be used in this application.

*Example 2:* $T_A$ = 85°C, $I_{OL}$ = 27.8 mA, $I_{OH}$ = 20 mA for each driver, $V_{CC}$ = 5.0 V, SOIC package. How many drivers per package can be used?

Maximum allowable power dissipation is:

$$PD_{max} = \frac{130°C - 85°C}{85°C/W} = 0.53\ W$$

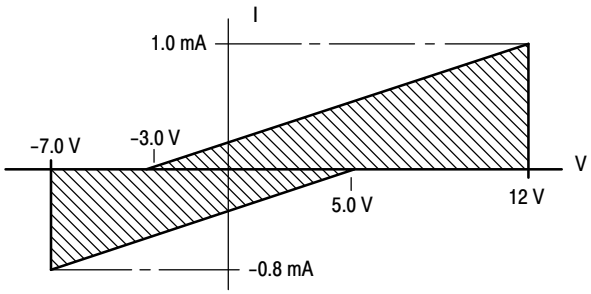
Since the power supply current of 60 mA dissipates 300 mW, that leaves 230 mW (530 mW − 300 mW) for the drivers. From Figures 8 and 10 (adjusted for $V_{CC}$ = 5.0 V), $V_{OL}$ ≈1.38 V, and $V_{OH}$ ≈4.27 V. The power dissipated in each driver is:

{(5.0 − 4.27) • 0.020} + (1.38 • 0.0278) = 53 mW

Since each driver dissipates 53 mW, the use of all four drivers in a package would be marginal. Options include reducing the load current, reducing the ambient temperature, and/or providing a heat sink.

### System Requirements

EIA−485 requires each driver to be capable of transmitting data differentially to at least 32 unit loads, plus an equivalent DC termination resistance of 60Ω, over a common mode voltage of −7.0 to 12 V. A unit load (U.L.), as defined by EIA−485, is shown in Figure 17.




Reprinted from EIA−485, Electronic Industries Association, Washington,DC.

**Figure 17. Unit Load Definition**

A load current within the shaded regions represents an impedance of less than one U.L., while a load current of a magnitude outside the shaded area is greater than one U.L. A system's total load is the sum of the unit load equivalents of each receiver's input current, and each disabled driver's output leakage current. The 60Ω termination resistance mentioned above allows for two 120Ω terminating resistors.

Using the EIA−485 requirements (worst case limits), and the graphs of Figures 7 and 9, it can be determined that the maximum current an MC75172B or MC75174B driver will source or sink is ≈65 mA.

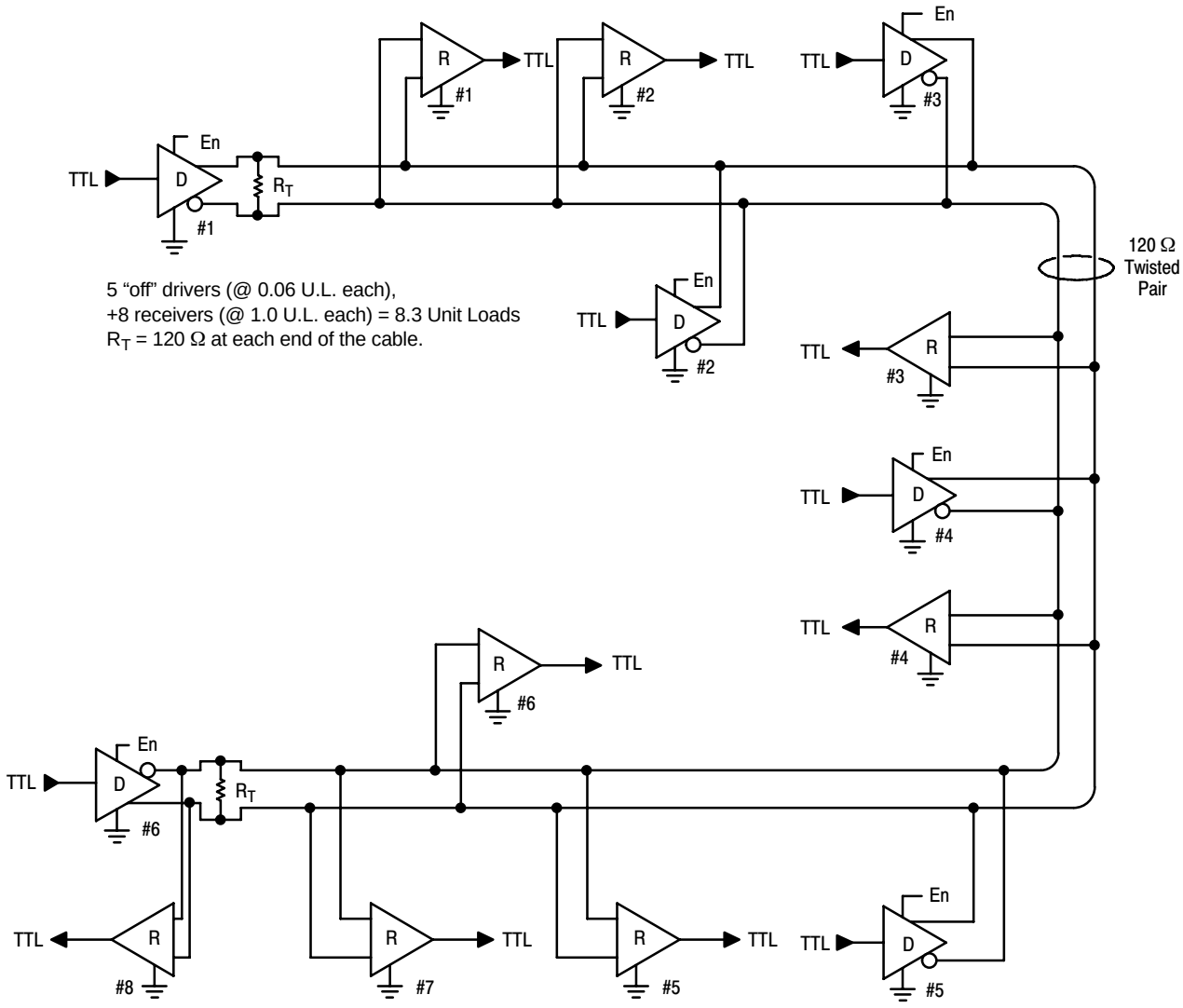
### System Example

An example of a typical EIA−485 system is shown in Figure 18. In this example, it is assumed each receiver's input characteristics correspond to 1.0 U.L. as defined in Figure 17. Each "off" driver, with a maximum leakage of ±50 μA over the common mode range, presents a load of ≈0.06 U.L. The total load for the active driver is therefore 8.3 unit loads, plus the parallel combination of the two terminating resistors (60Ω). It is up to the system software to control the driver Enable pins to ensure that only one driver is active at any time.

### Termination Resistors

Transmission line theory states that, in order to preserve the shape and integrity of a waveform traveling along a cable, the cable must be terminated in an impedance equal to its characteristic impedance. In a system such as that depicted in Figure 18, in which data can travel in both directions, both physical ends of the cable must be terminated. Stubs, leading to each receiver and driver, should be as short as possible.

Leaving off the terminations will generally result in reflections which can have amplitudes of several volts above $V_{CC}$ or below ground. These overshoots and undershoots can disrupt the driver and/or receiver operation, create false data, and in some cases damage components on the bus.




NOTES: 1. Terminating resistors $R_T$ must be located at the physical ends of the cable.
2. Stubs should be as short as possible.
3. Circuit ground of all drivers and receivers must be connected via a dedicated wire within the cable. Do not rely on chassis ground or power line ground.

**Figure 18. Typical EIA−485 System**

**COMPARING SYSTEM REQUIREMENTS**

| Characteristic | Symbol | EIA−485 | EIA−422−A | V.11 and X.27 |
|---|---|---|---|---|
| **GENERATOR (Driver)** | | | | |
| Output Impedance (Note 1) | $Z_{out}$ | Not Specified | < 100 Ω | 50 10 100 Ω |
| Open Circuit Voltage<br>Differential<br>Single−Ended | <br>$V_{OCD}$<br>$V_{OCS}$ | <br>1.5 to 6.0 V<br>< 6.0 V | <br>≤ 6.0 V<br>≤ 6.0 V | <br>≤ 6.0 V, w/3.9 kΩ, Load<br>≤ 6.0 V, w/3.9 kΩ, Load |
| Loaded Differential Voltage | $V_{OD}$ | 1.5 to 5.0 V, w/54 Ω load | ≥ 2.0 V or ≥ 0.5 $V_{OCD}$, w/100 Ω load | ≥ 2.0 V or ≥ 0.5 $V_{OCD}$, w/100 Ω load |
| Differential Voltage Balance | $\Delta V_{OD}$ | < 200 mV | ≤ 400 mV | < 400 mV |
| Output Common Mode Range | $V_{CM}$ | −7.0 to +12 V | Not Specified | Not Specified |
| Offset Voltage | $V_{OS}$ | −1.0 < $V_{OS}$ < 3.0 V | ≤ 3.0 V | ≤ 3.0 V |
| Offset Voltage Balance | $\Delta V_{OS}$ | < 200 mV | ≤ 400 mV | < 400 mV |
| Short Circuit Current | $I_{OS}$ | ≤ 250 mA for −7.0 to 12 V | ≤ 150 mA to ground | ≤ 150 mA to ground |
| Leakage Current ($V_{CC}$ = 0) | $I_{OLK}$ | Not Specified | ≤ 100 μA to −0.25 V thru 6.0 V | ≤ 100 μA to ± 0.25 V |
| Output Rise/Fall Time (Note 2) | $t_r$, $t_f$ | ≤ 0.3 $T_B$, w/54 Ω/1150 pF load | ≤ 0.1 $T_B$ or ≤ 20 ns, w/100 Ω load | ≤ 0.1 $T_B$ or ≤ 20 ns, w/100 Ω load |
| **RECEIVER** | | | | |
| Input Sensitivity | $V_{th}$ | ± 200 mV | ± 200 mV | ± 300 mV |
| Input Bias Voltage | $V_{bias}$ | ≤ 3.0 V | ≤ 3.0 V | ≤ 3.0 V |
| Input Common Mode Range | $V_{cm}$ | −7.0 to 12 V | −7.0 to 7.0 V | −7.0 to 7.0 V |
| Dynamic Input Impedance | $R_{in}$ | Spec number of U.L. | ≥ 4 kΩ | ≥ 4 kΩ |

NOTES: 1. Compliance with V.11 and X.27 (Blue book) output impedance requires external resistors in series with the outputs of the MC75172B and MC75174B.
2. $T_B$ = Bit time.

### Additional Information

Copies of the EIA Recommendations (EIA−485 and EIA−422−A) can be obtained from the Electronics Industries Association, Washington, D.C. (202−457−4966). Copies of the CCITT Recommendations (V.11 and X.27) can be obtained from the United States Department of Commerce, Springfield, VA (703−487−4600).

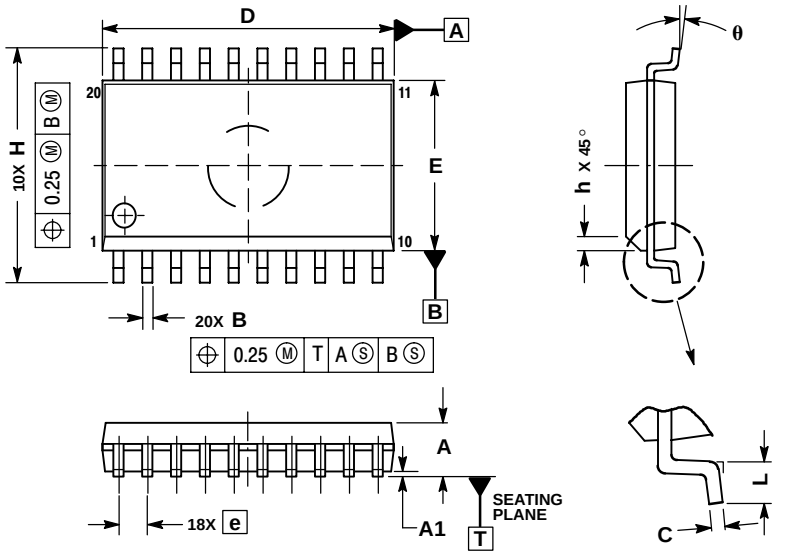
**ORDERING INFORMATION**

| Device | Operating Temperature Range | Package | Shipping† |
|---|---|---|---|
| MC75172BDW | $T_A$ = −40° to +85°C | SOIC−20WB | 38 Units / Rail |
| MC75172BDWG | | SOIC−20WB (Pb−Free) | |
| MC75172BDWR2 | | SOIC−20WB | 1000 / Tape & Reel |
| MC75172BDWR2G | | SOIC−20WB (Pb−Free) | |
| MC75174BDW | | SOIC−20WB | 38 Units / Rail |
| MC75174BDWG | | SOIC−20WB (Pb−Free) | |
| MC75174BDWR2 | | SOIC−20WB | 1000 / Tape & Reel |
| MC75174BDWR2G | | SOIC−20WB (Pb−Free) | |
| MC75174BP | | PDIP−16 | 25 Units / Rail |
| MC75174BPG | | PDIP−16 (Pb−Free) | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

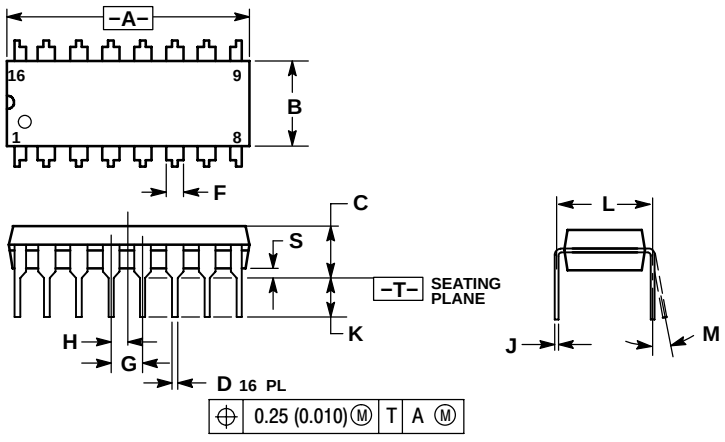
**SOIC−20 WB**
**DW SUFFIX**
**PLASTIC PACKAGE**
**CASE 751D−05**
**ISSUE G**




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

**PDIP−16**
**P SUFFIX**
**PLASTIC PACKAGE**
**CASE 648−08**
**ISSUE T**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |