24C16-SMD

◇ STRUCTURE Silicon Monolithic Integrated Circuit

◇ PRODUCT I^2C BUS Serial EEPROMs

◇ SERIES ADVANTAGE SERIES

◇ FAMILY BR24C□□ family

◇ TYPE Supply voltage 2.7V～5.5V/Opreating temperature -40℃～+85℃type

◇ PART NUMBER BR24C□□-10□U-2.7

PART NUMBER	PACKAGE	DENSITY
BR24C01A -10SU-2.7	8-lead JEDECSOIC	1Kbit
BR24C02N -10SU-2.7		2Kbit
BR24C04N -10SU-2.7		4Kbit
BR24C08AN -10SU-2.7		8Kbit
BR24C16AN -10SU-2.7		16Kbit
BR24C32AN -10SU-2.7		32Kbit
BR24C64AN -10SU-2.7		64Kbit
BR24C01A -10TU-2.7	8-lead TSSOP	1Kbit
BR24C02 -10TU-2.7		2Kbit
BR24C04 -10TU-2.7		4Kbit
BR24C08A -10TU-2.7		8Kbit
BR24C16A -10TU-2.7		16Kbit
BR24C32A -10TU-2.7		32Kbit

◇ FEATURE

Two wire serial interface
Endurance : 1,000,000 erase/write cycles
Data retention : 100years
Intial Data FFh in all address

◇ ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Operating Temperature	Topr	-40～85	℃
Storage Temperature	Tstg	-65～125	℃
Voltage on Any Pin with Respect to Ground	-	-0.3～Vcc+0.3	V
Maximum Operating Voltage	Vcc	-0.3～6.5	V

◇ POWER DISSIPATION (Ta=25℃)

PACKAGE	Rating	Unit
8-lead JEDECSOIC	450 *1	mW
8-lead TSSOP	330 *2	mW

* Degradation is done at 4.5mW/℃(*1), 3.3mW/℃(*2)for operation above 25℃

◇ DC OPERATING CHARACTERISTICS

BR24C01A/02/04/08A/16A.Unless otherwise specified.Vcc=2.7V to 5.5V, Ta=-40℃ to 85℃

Parameter	Symbol	Min	Max	Unit	Test Conditions
Supply Current Vcc=5.0V	I_{CC1}	–	1.0	mA	READ at 100 kHz
Supply Current Vcc=5.0V	I_{CC2}	–	3.0	mA	WRITE at 100 kHz
Standby Current Vcc=2.7V	I_{SB1}	–	4.0	μA	$V_{IN}=V_{CC}$ or GND
Standby Current Vcc=5.0V	I_{SB2}	–	18.0	μA	$V_{IN}=V_{CC}$ or GND
Input Leakage Current	I_{LI}	–	3.0	μA	$V_{IN}=V_{CC}$ or GND
Output Leakage Current	I_{LO}	–	3.0	μA	$V_{OUT}=V_{CC}$ or GND
Input Low Level	V_{IL}	–	Vccx0.3	V	-
Input High Level	V_{IH}	Vccx0.7	-	V	-
Output Low Level Vcc=3.0V	V_{OL}	–	0.4	V	I_{OL}=2.1mA

BR24C32A/64A Unless otherwise specified.Vcc=2.7V to 5.5V, Ta=-40℃ to 85℃

Parameter	Symbol	Min	Max	Unit	Test Conditions
Supply Current Vcc=5.0V	I_{CC1}	–	1.0	mA	READ at 400 kHz
Supply Current Vcc=5.0V	I_{CC2}	–	3.0	mA	WRITE at 400 kHz
Standby Current Vcc=2.7V	I_{SB1}	–	2.0	μA	$V_{IN}=V_{CC}$ or GND
Standby Current Vcc=5.0V	I_{SB2}	–	6.0	μA	$V_{IN}=V_{CC}$ or GND
Input Leakage Current	I_{LI}	–	3.0	μA	$V_{IN}=V_{CC}$ or GND
Output Leakage Current	I_{LO}	–	3.0	μA	$V_{OUT}=V_{CC}$ or GND
Input Low Level	V_{IL}	–	Vccx0.3	V	-
Input High Level	V_{IH}	Vccx0.7	-	V	-
Output Low Level Vcc=3.0V	V_{OL}	–	0.4	V	I_{OL}=2.1mA

OThis product is not designed for protection against radioactive rays.

* Degradation is done at 4.5mW/℃(*1), 3.3mW/℃(*2)for operation above 25℃

◇ AC OPERATING CHARACTERISTICS

BR24C01A/02/04/08A/16A.Unless otherwise specified.Vcc=2.7V to 5.5V, Ta=-40℃ to 85℃

Parameter	Symbol	2.7, 5.0V		Unit
		Min	Max	
Clock Frequency, SCL	f_{SCL}	-	400	kHz
Clock Pulse Width Low	t_{LOW}	1.2	-	μs
Clock Pulse Width High	t_{HIGH}	0.6	-	μs
Noise Suppression Time	t_I	-	50	ns
Clock Low to Data Out Valid	t_{AA}	0.1	0.9	μs
Time the bus must be free before a new transmission can start	t_{BUF}	1.2	-	μs
Start Hold Time	$t_{HD.STA}$	0.6	-	μs
Start Setup Time	$t_{SU.STA}$	0.6	-	μs
Data In Hold Time	$t_{HD.DAT}$	0	-	μs
Data In Setup Time	$t_{SU.DAT}$	100	-	ns
Inputs Rise Time *1	t_R	-	0.3	μs
Inputs Fall Time *1	t_F	-	300	ns
Stop Setup Time	$t_{SU.STO}$	0.6	-	μs
Data Out Hold Time	t_{DH}	50	-	ns
Write Cycle Time	t_{WR}	-	5	ms
Endurance *1 5.0V, 25℃	Endurance	1M	-	Write Cycles

*1 Not 100% TESTED

BR24C32A/64A Unless otherwise specified.Vcc=2.7V to 5.5V, Ta=-40℃ to 85℃

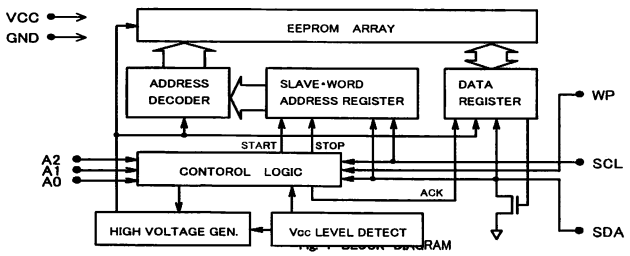
Parameter	Symbol	2.7-5.0V		Unit
		Min	Max	
Clock Frequency, SCL	f_{SCL}	-	400	kHz
Clock Pulse Width Low	t_{LOW}	1.3 *2	-	μs
		1.2 *3	-	
Clock Pulse Width High	t_{HIGH}	0.6	-	μs
Noise Suppression Time	t_I	-	50	ns
Clock Low to Data Out Valid	t_{AA}	0.1	0.9	μs
Time the bus must be free before a new transmission can start	t_{BUF}	1.3 *2	-	μs
		1.2 *3	-	
Start Hold Time	$t_{HD.STA}$	0.6	-	μs
Start Setup Time	$t_{SU.STA}$	0.6	-	μs
Data In Hold Time	$t_{HD.DAT}$	0	-	μs
Data In Setup Time	$t_{SU.DAT}$	100	-	ns
Inputs Rise Time *1	t_R	-	0.3	μs
Inputs Fall Time *1	t_F	-	300	ns
Stop Setup Time	$t_{SU.STO}$	0.6	-	μs
Data Out Hold Time	t_{DH}	50	-	ns
Write Cycle Time	t_{WR}	-	5	ms
Endurance *1 5.0V, 25℃	Endurance	1M	-	Write Cycles

*1 Not 100% TESTED

*2 BR24C32A

*3 BR24C64A

◇ BLOCK DIAGRAM



◇ PIN No., PIN NAME

PIN No.	PIN NAME
1	A0
2	A1
3	A2
4	GND
5	SDA
6	SCL
7	WP
8	Vcc

◇NOTES FOR POWER SUPPLY

Vcc rises through the low voltage region in which internal circuit of IC and the controller are unstable, so that device may not work properly due to an incomplete reset of internal circuit. To prevent this, the device has the feature of P.O.R. and LVCC. In the case of power up, keep the following conditions to ensure functions of P.O.R. and LVCC.

1. It is necessary to be "SDA='H'" and "SCL='L' or 'H'".
2. Follow the recommended conditions of tR, tOFF, Vbot for the function of P.O.R. during power up.

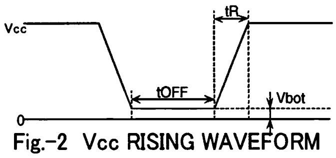


Fig.-2 Vcc RISING WAVEFORM

◇RECOMMENDED CONDITIONS OF tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

3. Prevent SDA and SCL from being "High-Z".
   In case that condition 1. and/or 2. cannot be met, take following actions.
   A) Unable to keep condition 1.
      (SDA is "LOW" during power up.)
      → Control SDA ,SCL to be "HIGH" as Fig.-3(a), 3(b).
   B) Unable to keep condition 2.
      → After power becomes stable, execute software reset.
   C) Unable to keep both conditions 1 and 2.
      → Follow the instruction A first, then the instruction B.

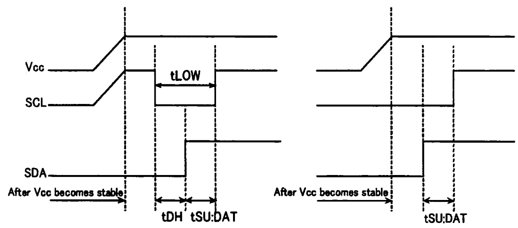


Fig.-3(a) SCL='H' and SDA='L' Fig.-3(b) SCL='L' and SDA='L'

◇CAUTIONS ON USE

(1) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

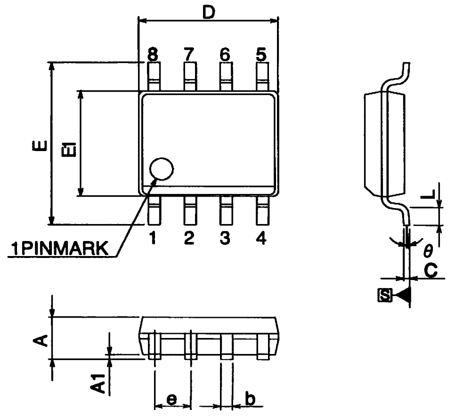
(2) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(3) Thermal design
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(4) Terminal to terminal shortcircuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(5) Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

◇ PHYSICAL DIMENSION

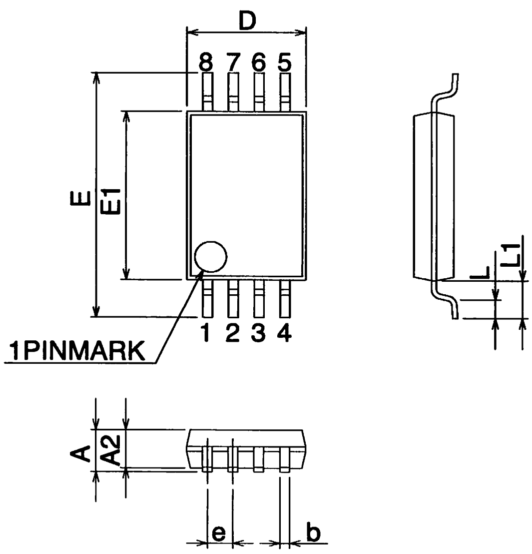


Notes
1.This drawing is subject to change without notice.
2.Body dimensions do not include mold flash or protrusion, or gate burns.
3.Reference JEDEC MS-012 variation AA.

Fig-4 8-lead JEDECSOIC Package Outline

◇ 8-lead JEDECSOIC Package Size Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	1.35	1.75	-	0.053	0.069
A1	-	0.10	0.25	-	0.004	0.010
b	-	0.31	0.51	-	0.012	0.020
c	-	0.17	0.25	-	0.007	0.010
D	-	4.80	5.00	-	0.189	0.197
e	1.27 BSC	-	-	0.050 BSC	-	-
E	-	5.79	6.20	-	0.228	0.244
E1	-	3.81	3.99	-	0.150	0.157
L	-	0.40	1.27	-	0.016	0.050
θ	-	0°	8°	-	0°	8°



Notes
1.This drawing is subject to change without notice.
2.Body dimensions do not include mold flash or protrusion, or gate burns.
3.Reference MO-153

Fig-5 8-lead TSSOP Package Outline

◇ 8-lead TSSOP Package Size Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	-	1.20	-	-	0.047
A2	1.00	0.80	1.05	0.039	0.031	0.041
b	-	0.19	0.30	-	0.007	0.012
D	3.00	2.90	3.10	0.118	0.114	0.122
e	0.65 BSC	-	-	0.025	-	-
E	6.40 BSC	-	-	0.252	-	-
E1	4.40	4.30	4.50	0.173	0.169	0.177
L	0.60	0.45	0.75	0.023	0.017	0.030
L1	1.00 REF	-	-	0.039	-	-